Verifying Programs In Weak Memory Models With Persistency

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The Institute of Mathematical Sciences

Joint work with
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Mohamed Faouzi Atig
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Verifying Programs In Weak Memory Models With Persistency

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Outline

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- Concurrent Programs

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- Concurrent Programs
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- Persistency
- Verification

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Intel x86 model

- Verification

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- Concurrent Programs
- Weak Memory models
- Persistency
- Verification

Intel x86 model

Extending Intel-x86 Consistency and Persistency

Formalising the Semantics of Intel-x86 Memory Types and Non-temporal Stores

AZALEA RAAD, Imperial College London, United Kingdom
LUC MARANGET, Inria, France
VIKTOR VAFEIADIS, MPI-SWS, Germany

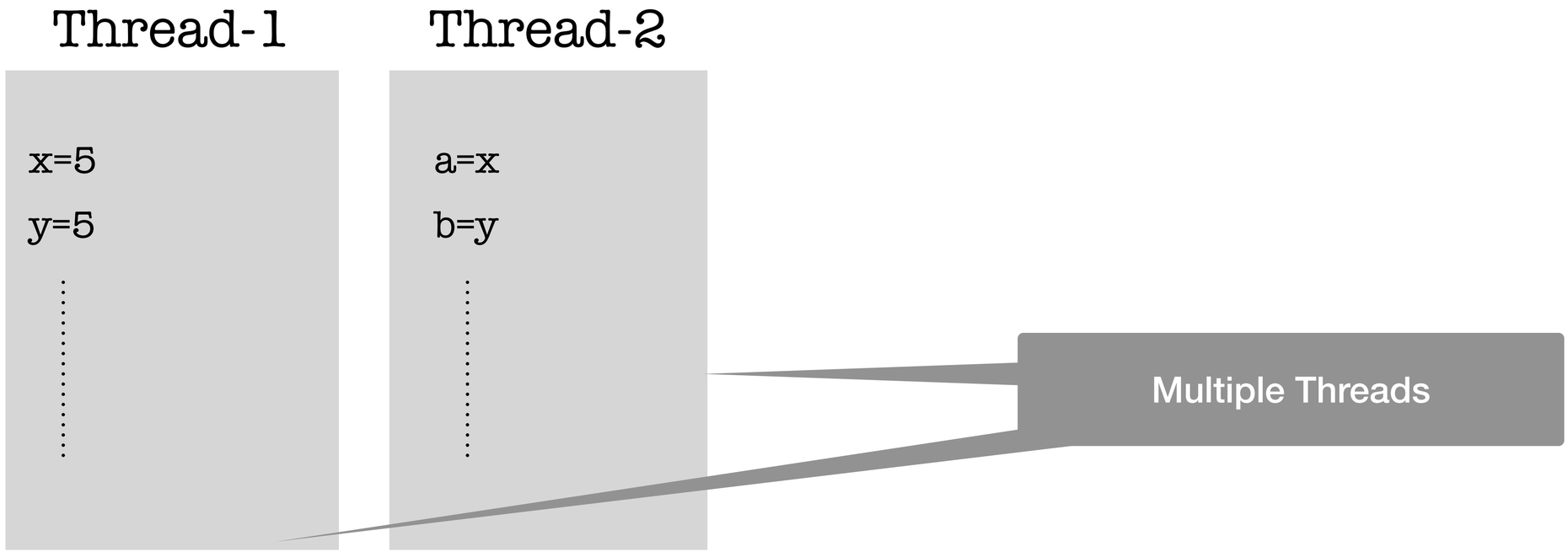
POPL 2022

CONCURRENT PROGRAMS

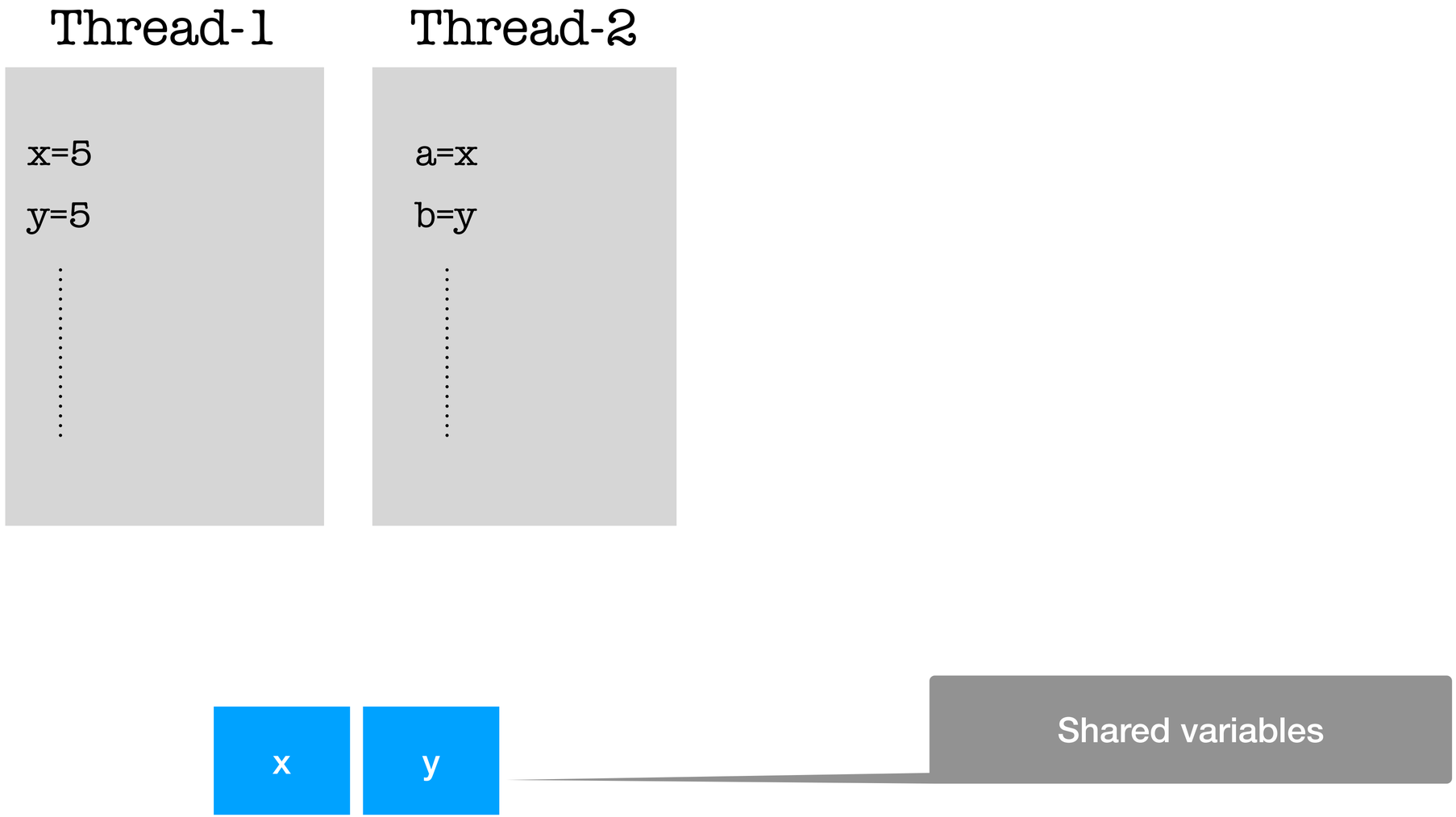
In the concurrent world, imperative is a wrong default - Tim Sweeny

Concurrent Programs

Concurrent Programs



Concurrent Programs



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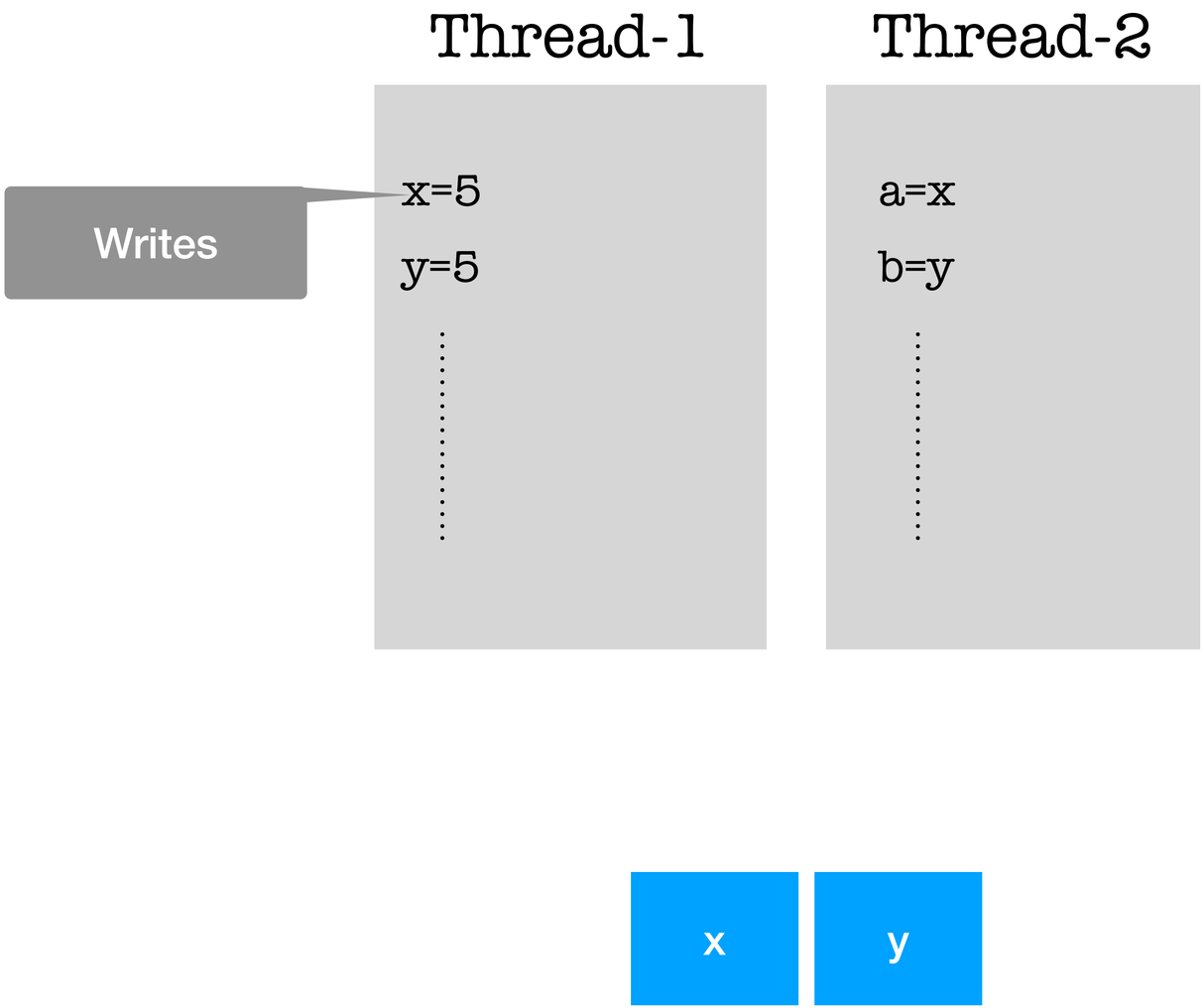
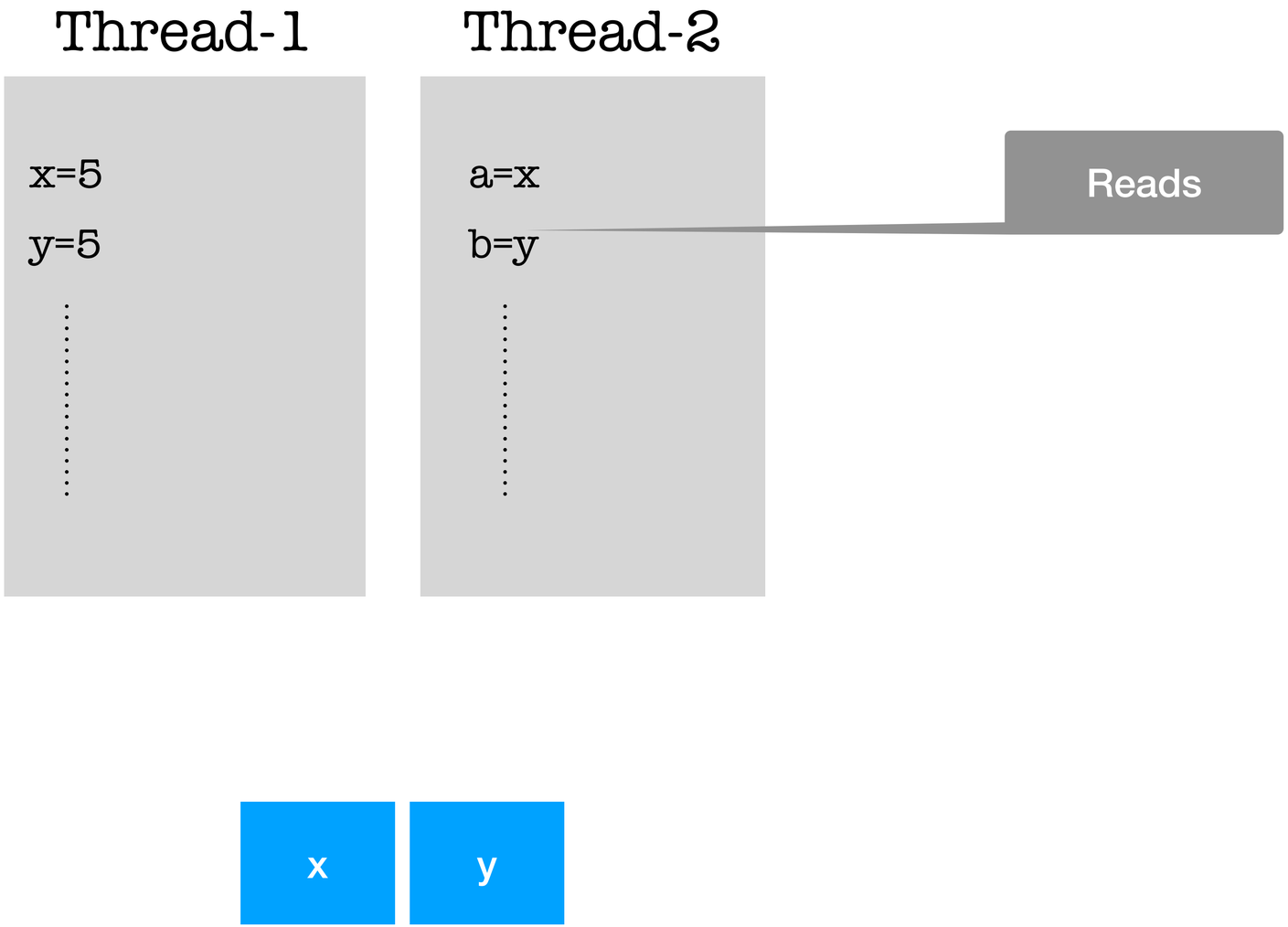
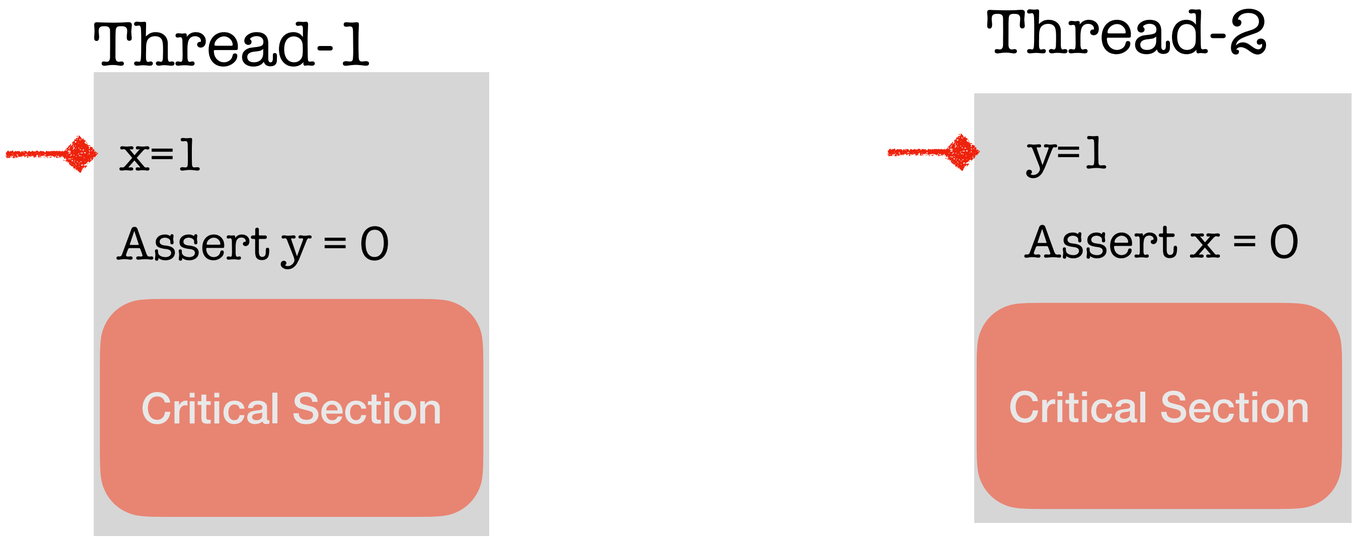
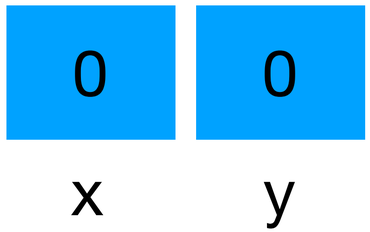


Concurrent Programs

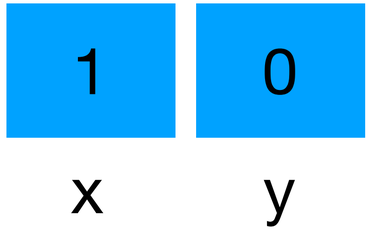


Dekker's Mutual Exclusion





Dekker's Mutual Exclusion



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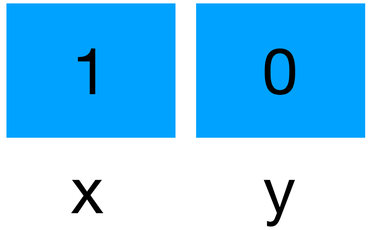
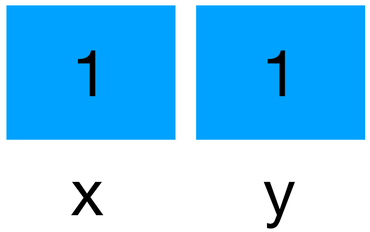


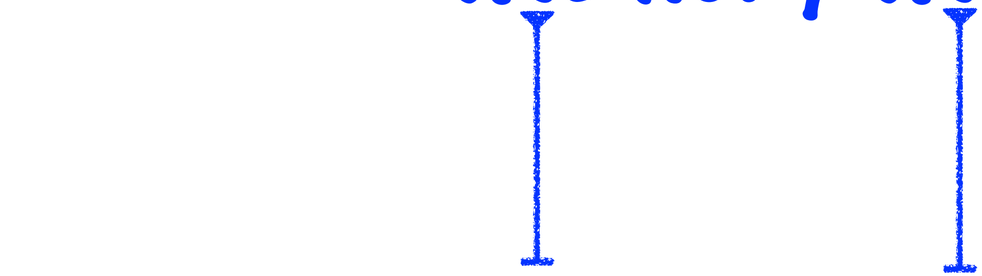
Dekker's Mutual Exclusion



WEAK MEMORY MODELS

don't communicate by sharing memory; share memory by communicating

Memory Models



Sequential Consistency

Weak Consistency

Memory Models

Sequential Consistency

Operations are atomic

Weak Consistency

Memory Models

Sequential Consistency

Operations are atomic

Weak Consistency

Operations can be re-ordered

Memory Models

Sequential Consistency

Operations are atomic

Weak Consistency

Operations can be re-ordered

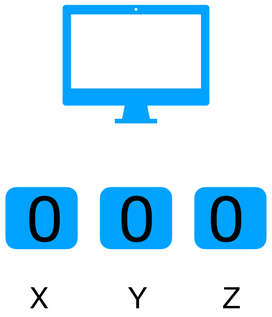
TSO, PSO, EX86

Sequential Consistency

Sequential Consistency

X Y Z

Sequential Consistency

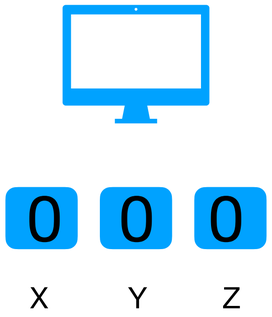


Instructions are sequential and immediate

Sequential Consistency

Instructions

Wr(x,1) Rd(y) RMW(z,0,2)



Instructions are sequential and immediate

Sequential Consistency

Instructions

Wr(x,1)

Rd(y)

RMW(z,0,2)

0 0 0

X Y Z

Sequential Consistency

Instructions

Wr(x,1)

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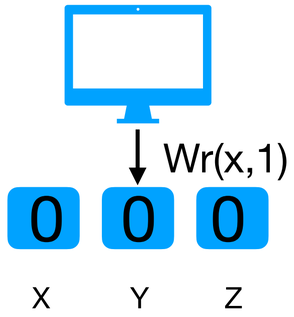


Write modifies the value of a variable

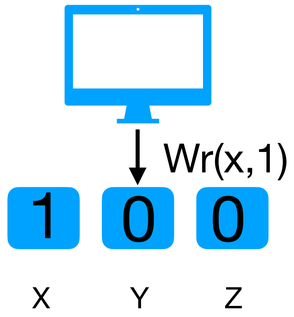
Sequential Consistency

Instructions

Wr(x,1)

Rd(y)

RMW(z,0,2)



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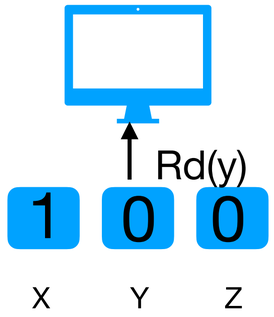
Wr(x,1) | Rd(y) | RMW(z,0,2)



Read fetches value of a variable

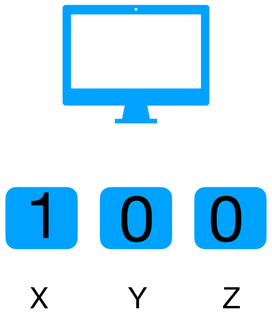
Sequential Consistency

Instructions

Wr(x,1)

Rd(y)

RMW(z,0,2)



Rmw tests and sets a variable

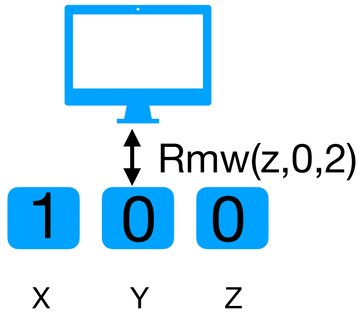
Sequential Consistency

Instructions

Wr(x,1)

Rd(y)

RMW(z,0,2)



Rmw tests and sets a variable

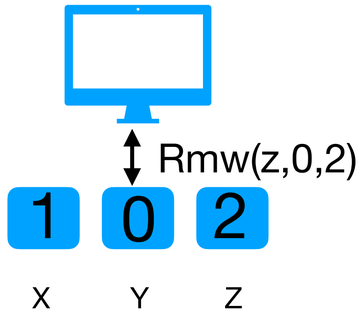
Sequential Consistency

Instructions

Wr(x,1)

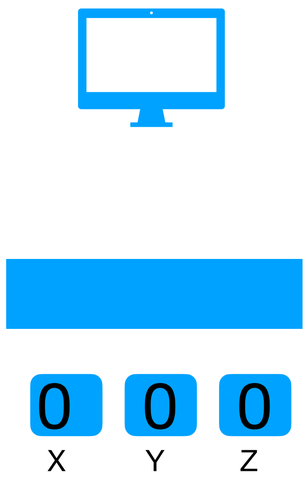
Rd(y)

RMW(z,0,2)

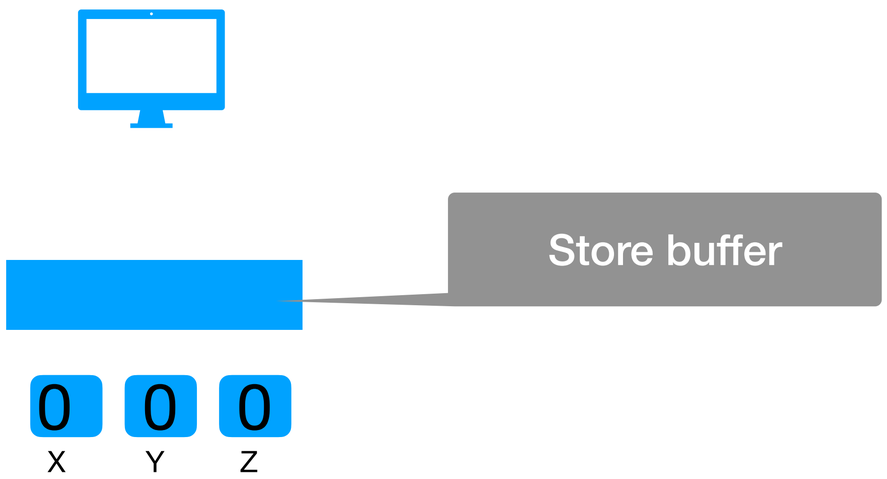


Rmw tests and sets a variable

Total Store Order



Total Store Order

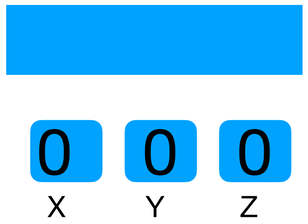


Writes are buffered, reads are immediate

Total Store Order

Instructions

Wr(x,d) Rd(x) Mf RMW(x,b,d)



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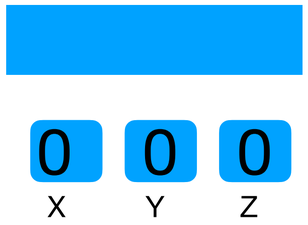

Total Store Order

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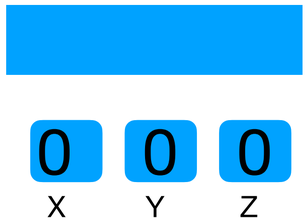

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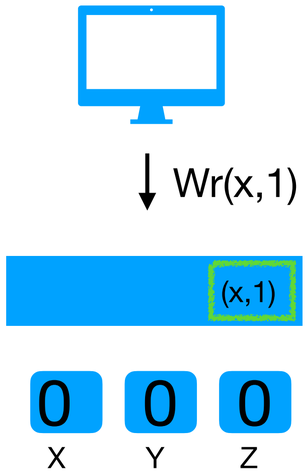


Writes are buffered

Total Store Order

Instructions

Wr(x,d) Rd(x) Mf RMW(x,b,d)

Wr(y,2)

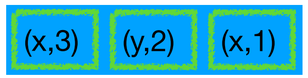
Writes are buffered

Total Store Order

Instructions

Wr(x,d) Rd(x) Mf RMW(x,b,d)

Wr(x,3)



Writes are buffered

Total Store Order

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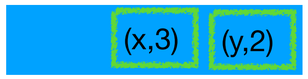

Propagated to memory non-deterministically

Total Store Order

Instructions

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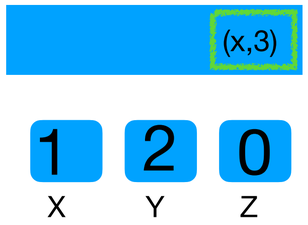

Propagated to memory non-deterministically

Total Store Order

Instructions

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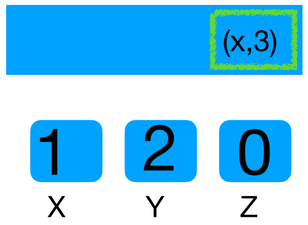


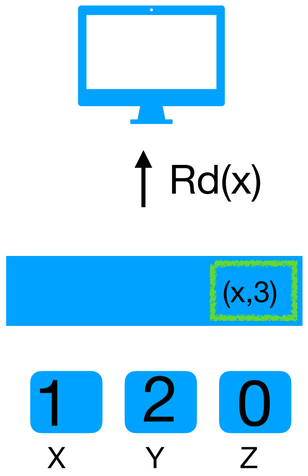
Reads are either from buffer or memory

In that order!!

Total Store Order

Instructions

Wr(x,d) | Rd(x) | Mf | RMW(x,b,d)



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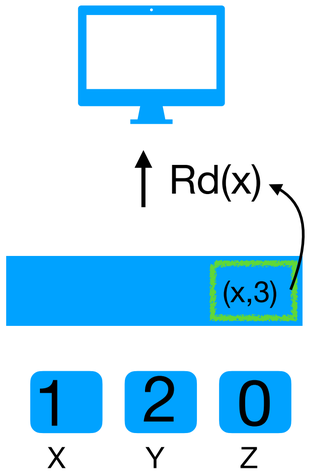

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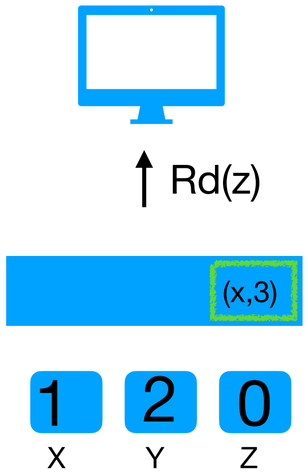

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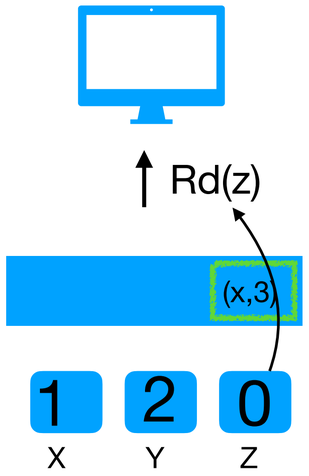

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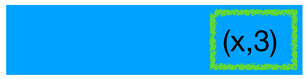

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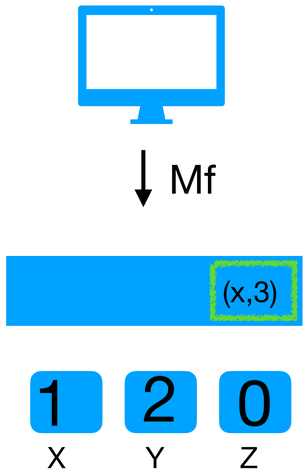
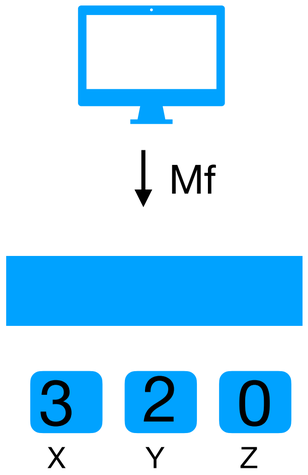


Memory fence ensures buffer is empty

Total Store Order

Instructions

Wr(x,d) Rd(x) Mf RMW(x,b,d)



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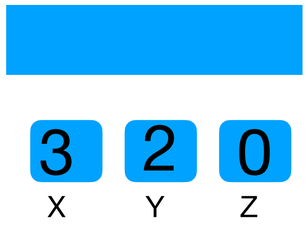
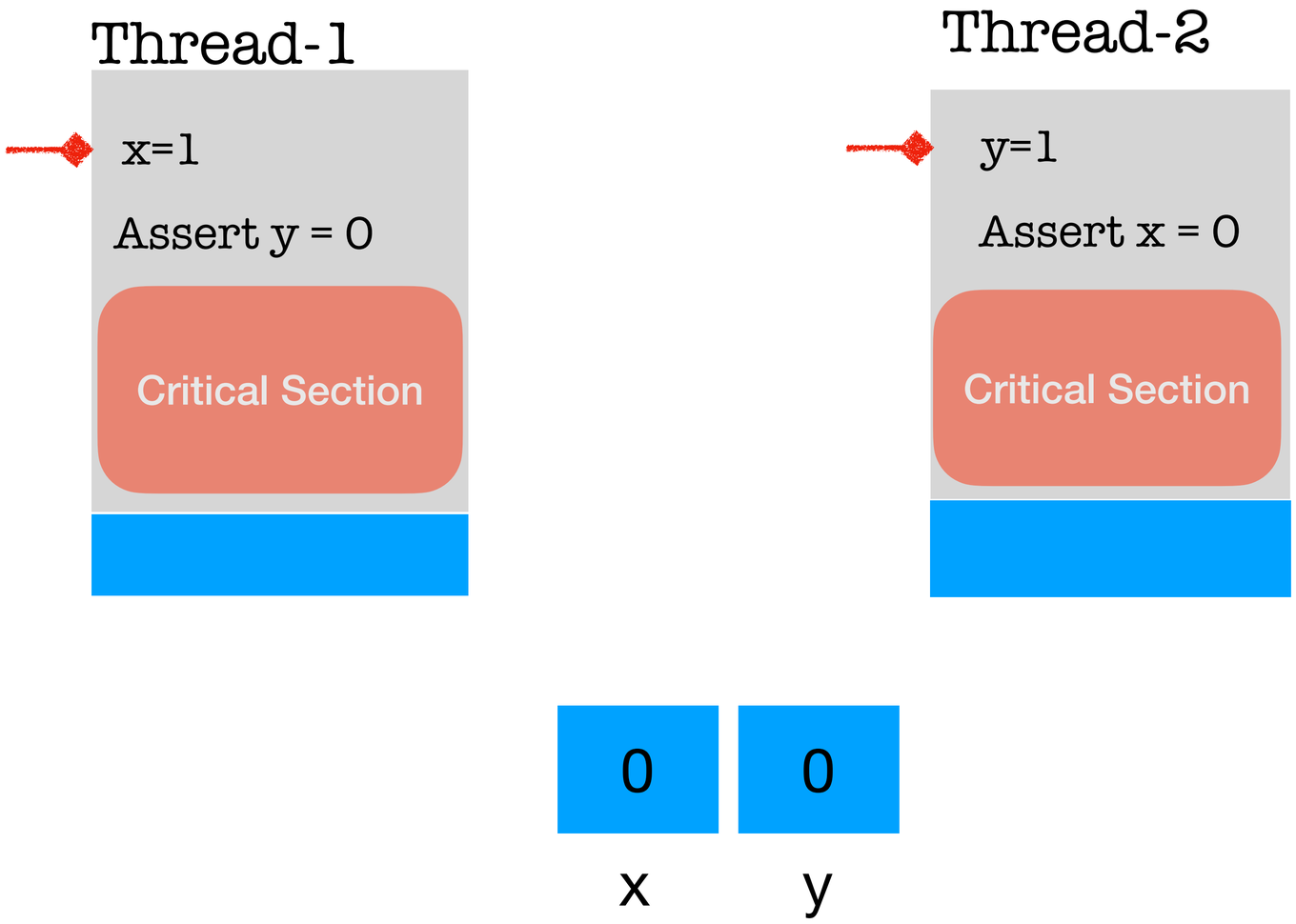
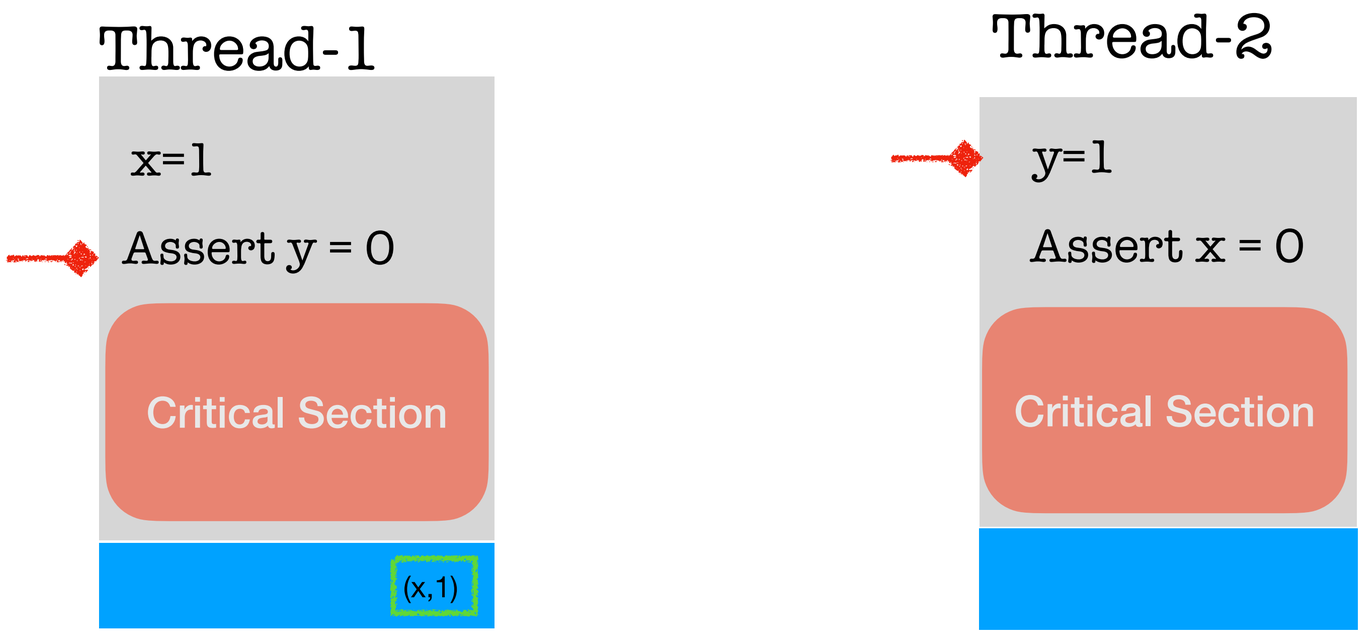


Memory fence ensures buffer is empty

Dekker's Mutual Exclusion



Dekker's Mutual Exclusion



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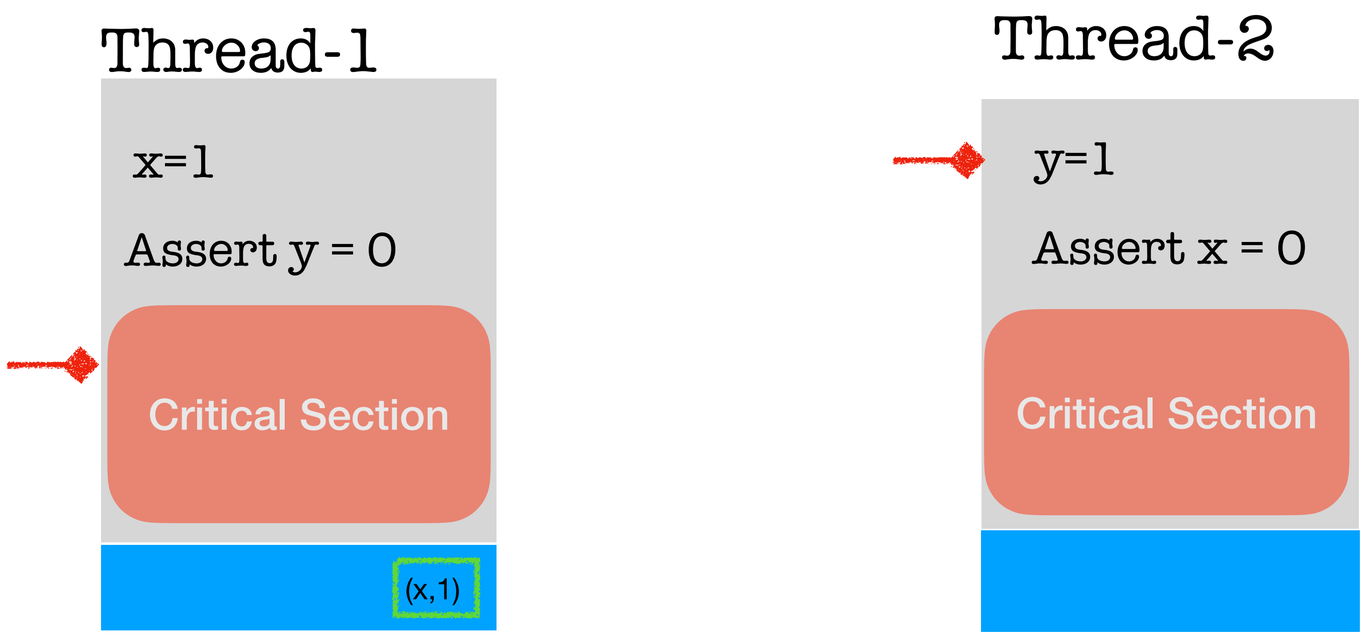

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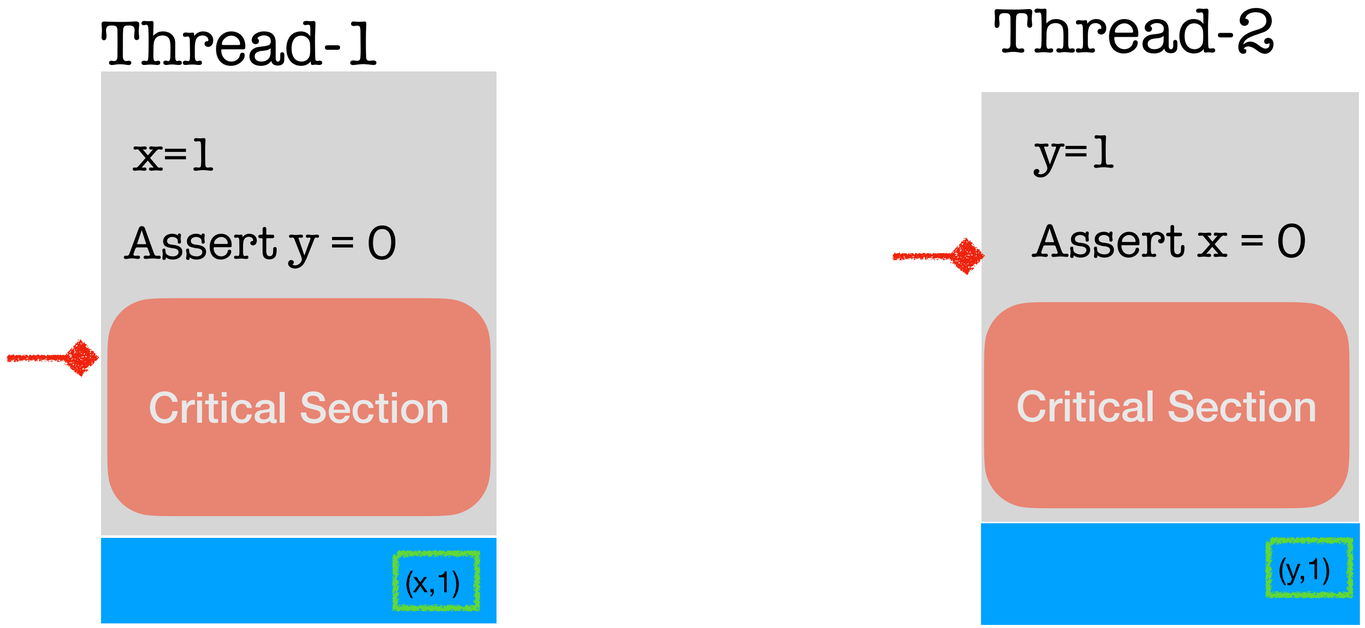

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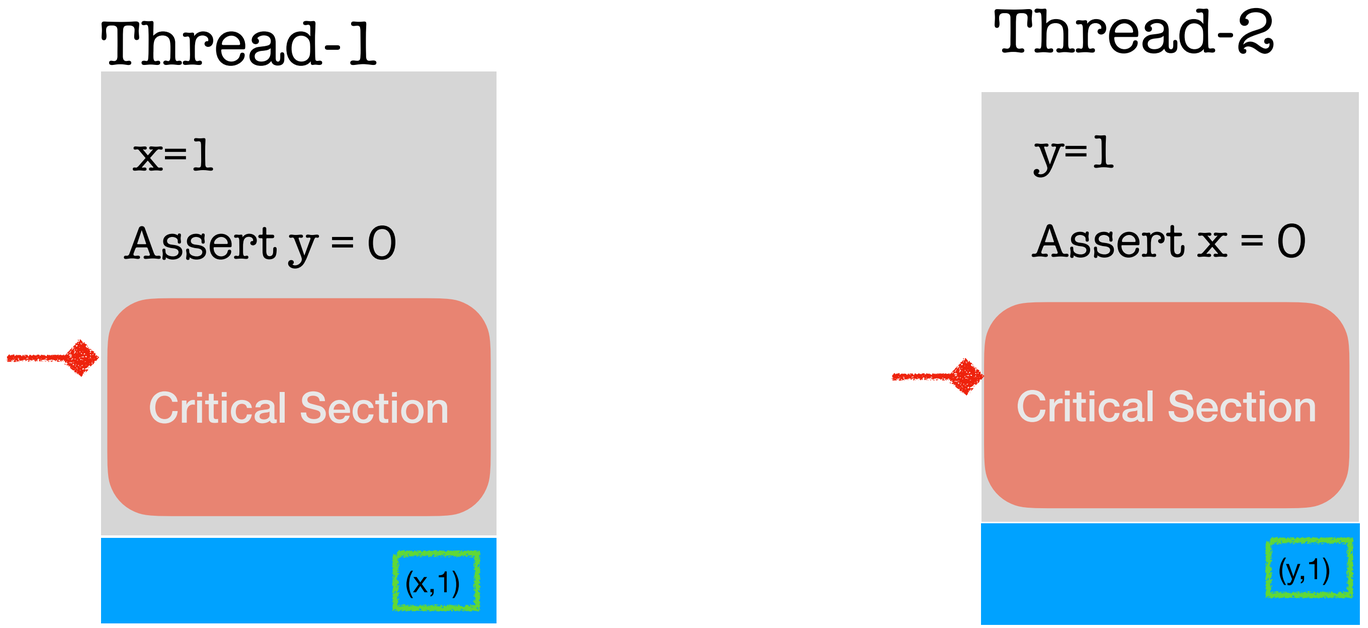
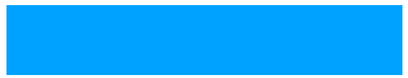


Partial Store Order

Instructions

Wr(x,d) Sf Rd(x) Mf Rmw(x,b,d)



0 0

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)

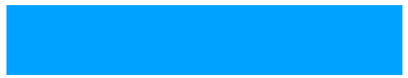
0 0

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)

Wr(x,1)



0 0

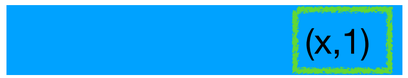
Writes are buffered

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)

Wr(x,1)



0 0

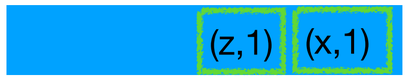
Writes are buffered

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)

Wr(z,1)



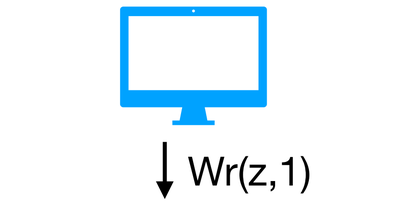
0 0

Writes are buffered

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)



0 0 0

X Y Z

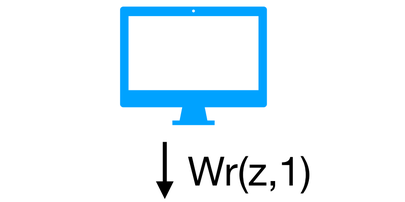
0 0

Propagated to memory non-deterministically

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)



0 0 0

X Y Z

0 0

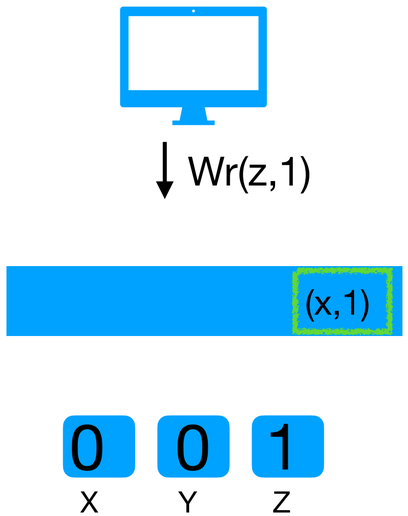
Propagated to memory non-deterministically

Reorders writes to different variables

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)



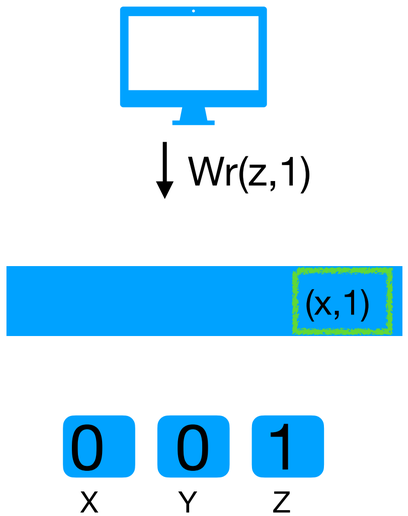
Propagated to memory non-deterministically

Reorders writes to different variables

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)

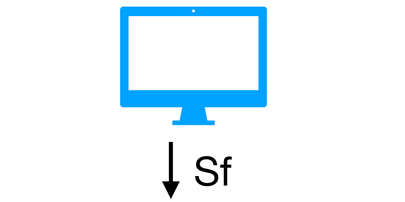


Store fence restricts re-ordering between writes

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)



0 0

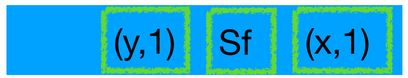
Store fence restricts re-ordering between writes

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)

Wr(y,1)



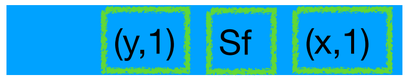
0 0

Store fence restricts re-ordering between writes

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)



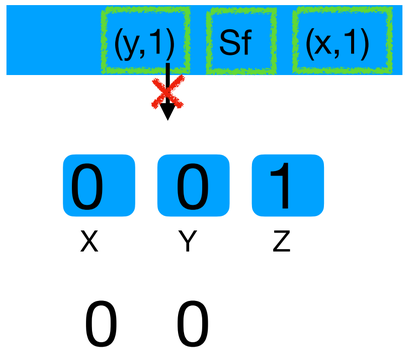
0 0

Store fence restricts re-ordering between writes

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)

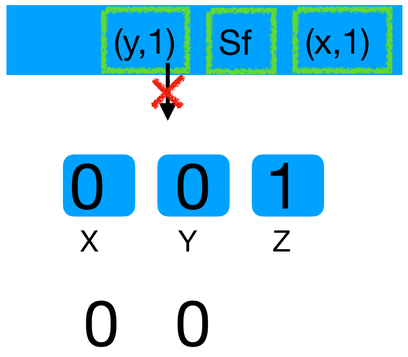


Store fence restricts re-ordering between writes

Partial Store Order

Instructions

Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)

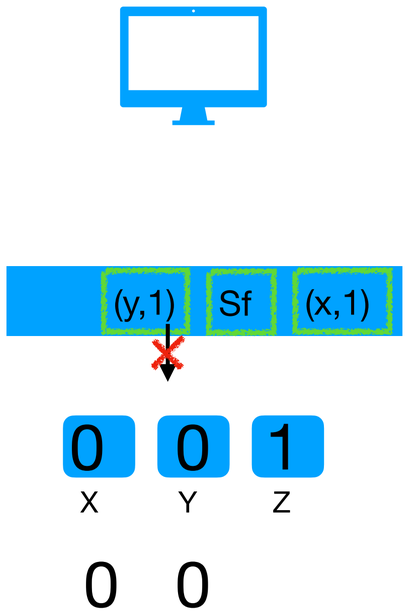


Store fence restricts re-ordering between writes

Partial Store Order

Instructions

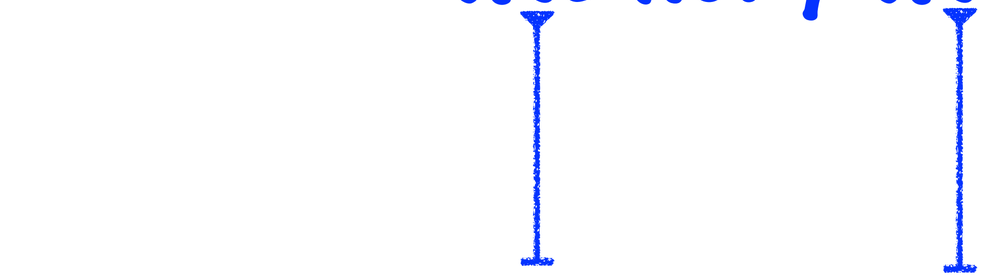
Wr(x,d) | Sf | Rd(x) | Mf | Rmw(x,b,d)



0 0

Store fence restricts re-ordering between writes

Memory Models



Sequential Consistency

Weak Consistency

Memory Models

Sequential Consistency

Atomic operations

Weak Consistency

Memory Models

Sequential Consistency

Atomic operations

Weak Consistency

Operations can be re-ordered

Memory Models

Sequential Consistency

Atomic operations

\+ Simple and intuitive

Weak Consistency

Operations can be re-ordered

Memory Models

Sequential Consistency

Atomic operations

+ Simple and intuitive

- Expensive

Weak Consistency

Operations can be re-ordered

Memory Models

Sequential Consistency

Atomic operations

+ Simple and intuitive

- Expensive

Weak Consistency

Operations can be re-ordered

+ Optimised for efficiency

Memory Models

Sequential Consistency

Atomic operations

+ Simple and intuitive

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Weak Consistency

Operations can be re-ordered

+ Optimised for efficiency

- Complicated

Memory Models

Sequential Consistency

Atomic operations

+ Simple and intuitive

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Weak Consistency

Operations can be re-ordered

+ Optimised for efficiency

- Complicated

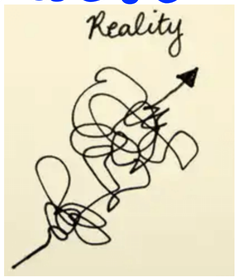
Memory Models

Sequential Consistency

Atomic operations

+ Simple and intuitive

- Expensive



Weak Consistency

Operations can be re-ordered

+ Optimised for efficiency

- Complicated

Extended x86 Explained

Extended x86 Explained

Instructions

Wb(x,d)

ntw(x,d)

Sf

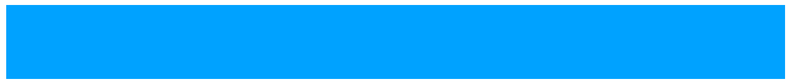
Fl(x)

Fo(x)

Rd(x)

Mf

Rmw(x,b,d)



Extended x86 Explained

Instructions

Wb(x,d)

ntw(x,d)

Sf

Fl(x)

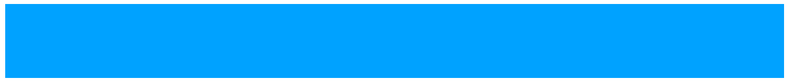
Fo(x)

Rd(x)

Mf

Rmw(x,b,d)

Writes are of type Ntw or Wb



Extended x86 Explained

Instructions

Wb(x,d)

ntw(x,d)

Sf

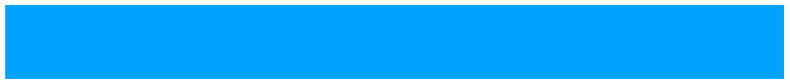
Fl(x)

Fo(x)

Rd(x)

Mf

Rmw(x,b,d)



Writes are of type Ntw or Wb

Original model has a complicated semantics with more kinds of writes.

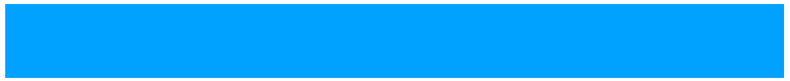
Extended x86 Explained

Instructions

Wb(x,d) ntw(x,d) Sf Fl(x) Fo(x)

Rd(x) Mf Rmw(x,b,d)

Writes are of type Ntw or Wb



Verification under Intel-x86 with Persistency

PAROSH ABDULLA, Uppsala University, Sweden
MOHAMED FAOUZI ATIG, Uppsala University, Sweden
AHMED BOUAJJANI, Université Paris Cité, France
K. NARAYAN KUMAR, Chennai Mathematical Institute and IRL ReLaX, India
PRAKASH SAIVASAN, Institute of Mathematical Sciences, HBNI and IRL ReLaX, India

For reachability, the two kinds of writes are sufficient

Extended x86 Explained

Instructions

Wb(x,d)

ntw(x,d)

Sf

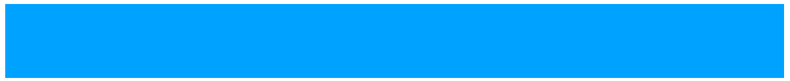
Fl(x)

Fo(x)

Rd(x)

Mf

Rmw(x,b,d)



Both types of writes are stored in buffer

Extended x86 Explained

Instructions

Wb(x,d)

ntw(x,d)

Sf

Fl(x)

Fo(x)

Rd(x)

Mf

Rmw(x,b,d)

0 0 0

X Y Z

Both types of writes are stored in buffer

Extended x86 Explained

Instructions

Wb(x,d) ntw(x,d) Sf Fl(x) Fo(x)

Rd(x) Mf Rmw(x,b,d)

Ntw writes re-order with writes of other variables

Extended x86 Explained

Instructions

Wb(x,d)

ntw(x,d)

Sf

Fl(x)

Fo(x)

Rd(x)

Mf

Rmw(x,b,d)

Wb writes do not re-order with each other

Extended x86 Explained

Instructions

Wb(x,d)

ntw(x,d)

Sf

Fl(x)

Fo(x)

Rd(x)

Mf

Rmw(x,b,d)

Wb writes do not re-order with each other

1 0 0

X Y Z

Extended x86 Explained

Instructions

Wb(x,d)

ntw(x,d)

Sf

Fl(x)

Fo(x)

Rd(x)

Mf

Rmw(x,b,d)

Wb writes do not re-order with each other

Extended x86 Explained

Instructions

Wb(x,d) ntw(x,d) Sf Fl(x) Fo(x)

Rd(x) Mf Rmw(x,b,d)

1 2 0

X Y Z

Fl, Sf disallows any re-orderings

Extended x86 Explained

Instructions

Wb(x,d) ntw(x,d) Sf Fl(x) Fo(x)

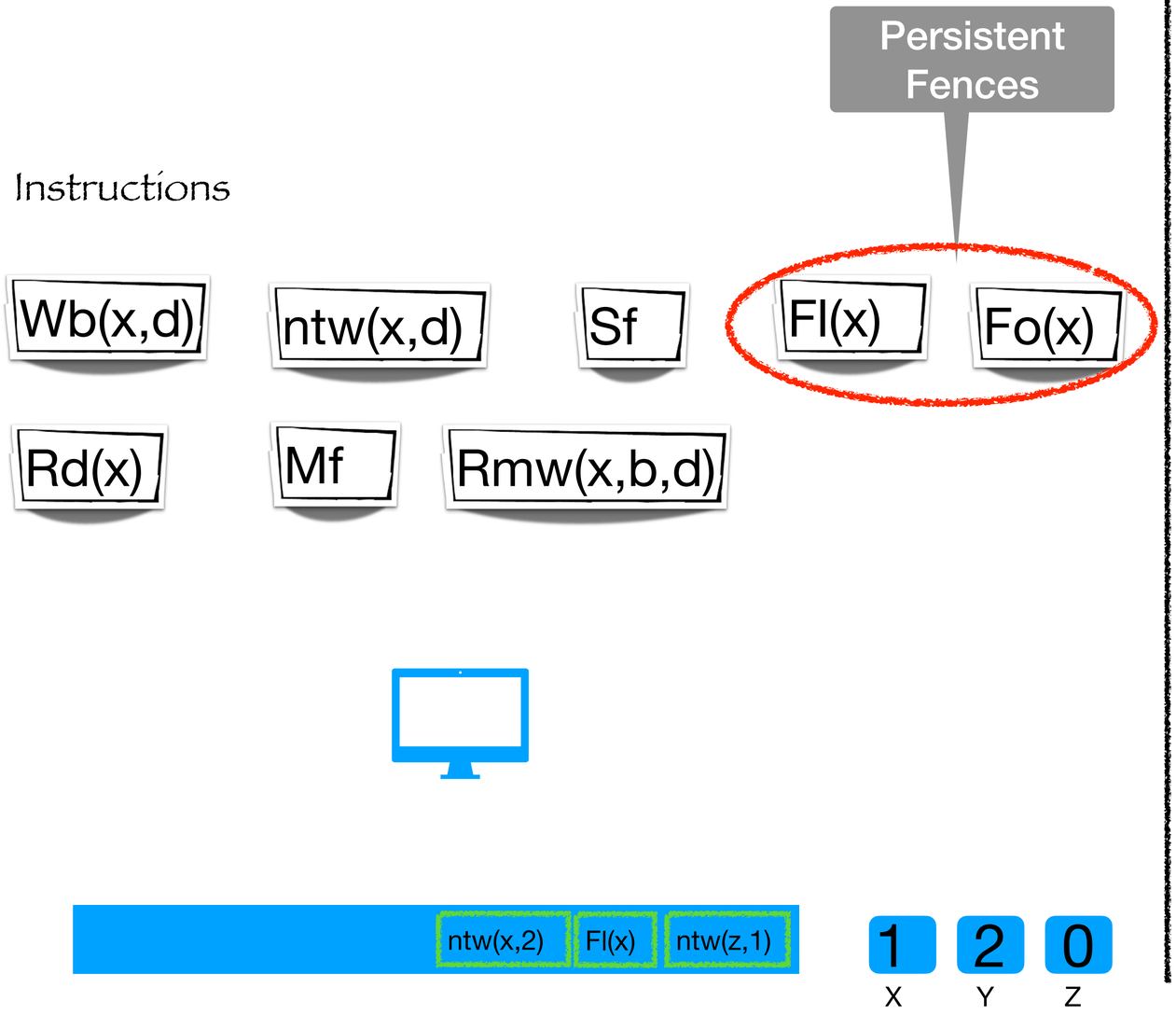
Rd(x) Mf Rmw(x,b,d)

1 2 0

X Y Z

Fo(x) cannot re-order with Sf and earlier writes to x

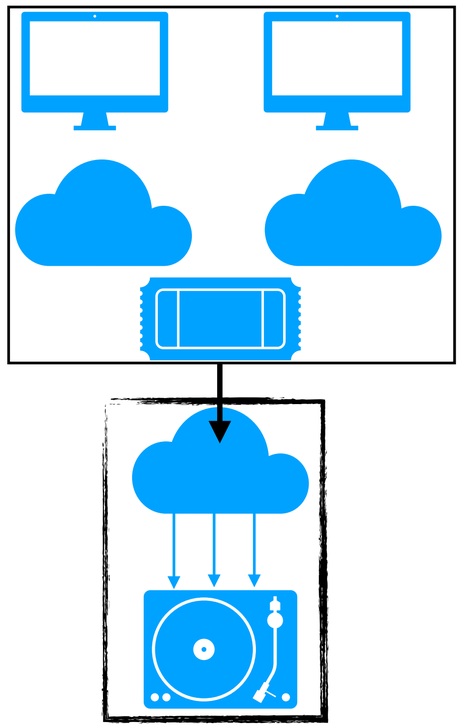
Extended x86 Explained



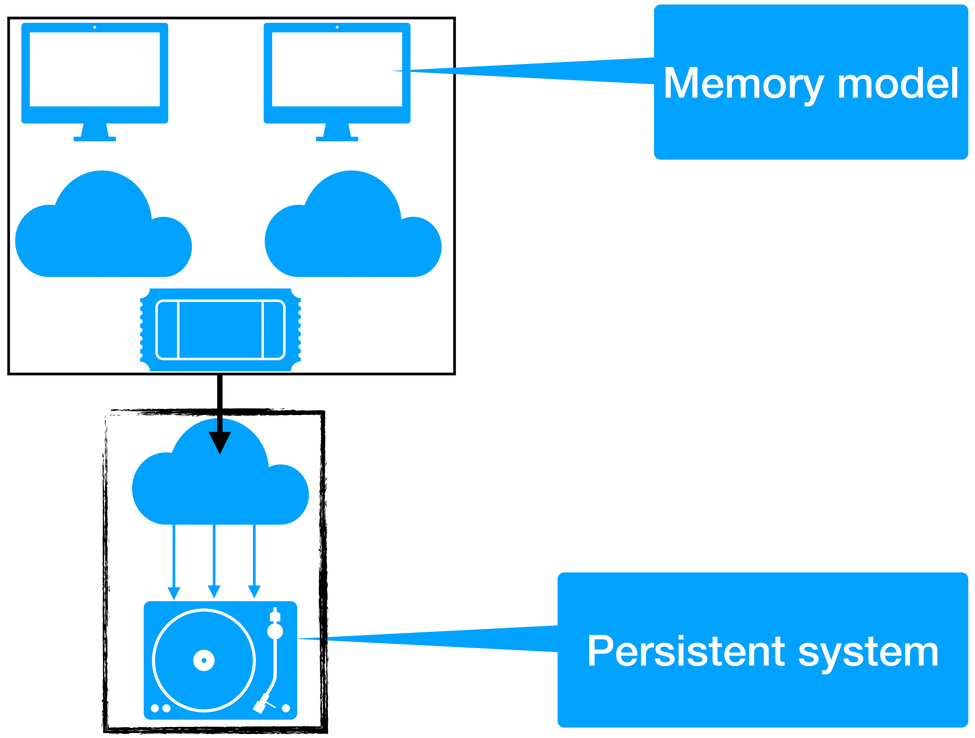
PERSISTENCY

Energy and persistence conquer all things - Benjamin Franklin

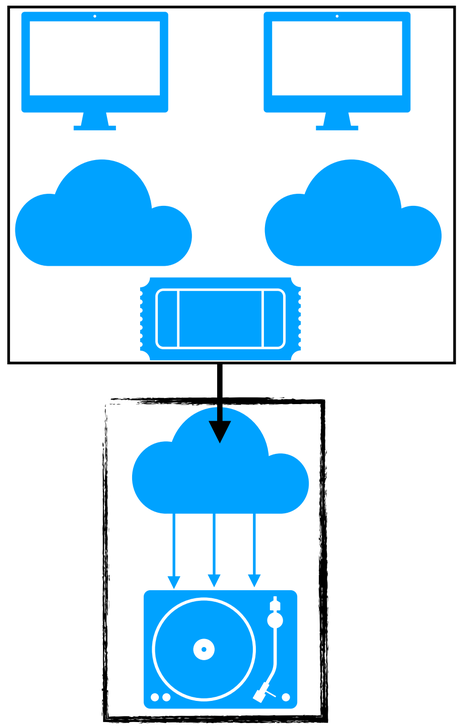
Concurrent Memory Systems + Persistency



Concurrent Memory Systems + Persistency

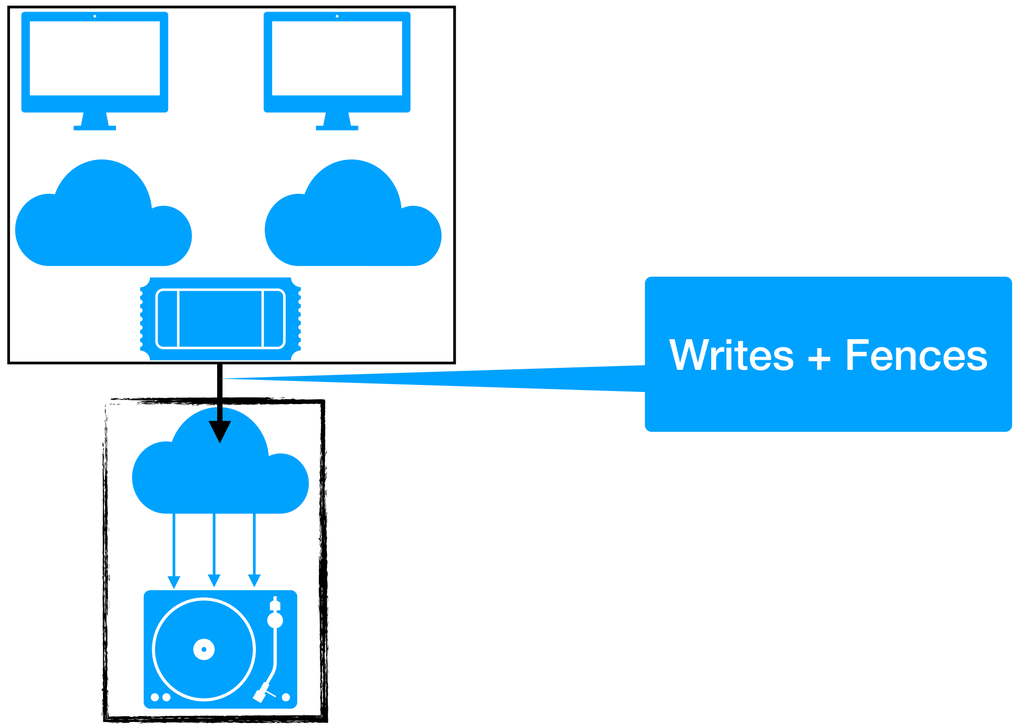


Concurrent Memory Systems + Persistency



Persistency

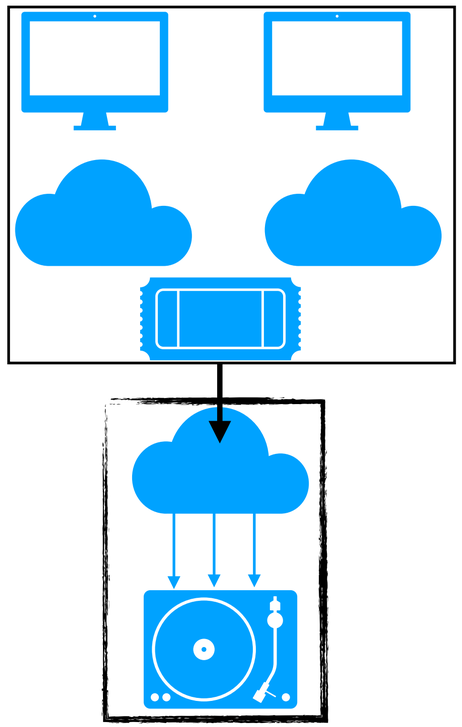
Concurrent Memory Systems + Persistency



Persistency

Archives writes, not necessarily in order

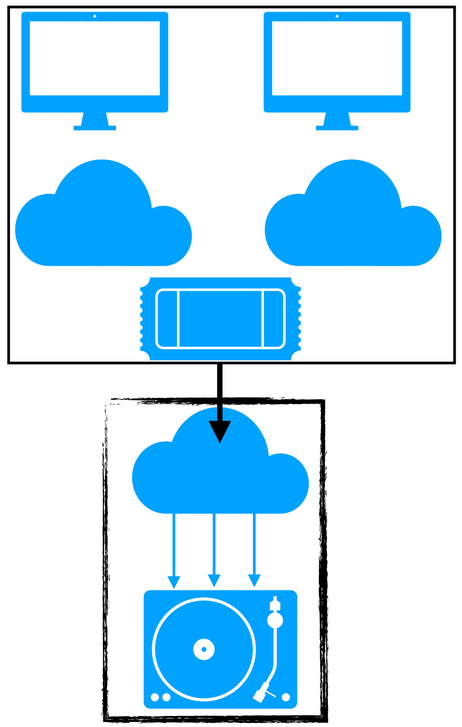
Concurrent Memory Systems + Persistency



Persistency

- Archives writes, not necessarily in order
- Re-orders incoming writes

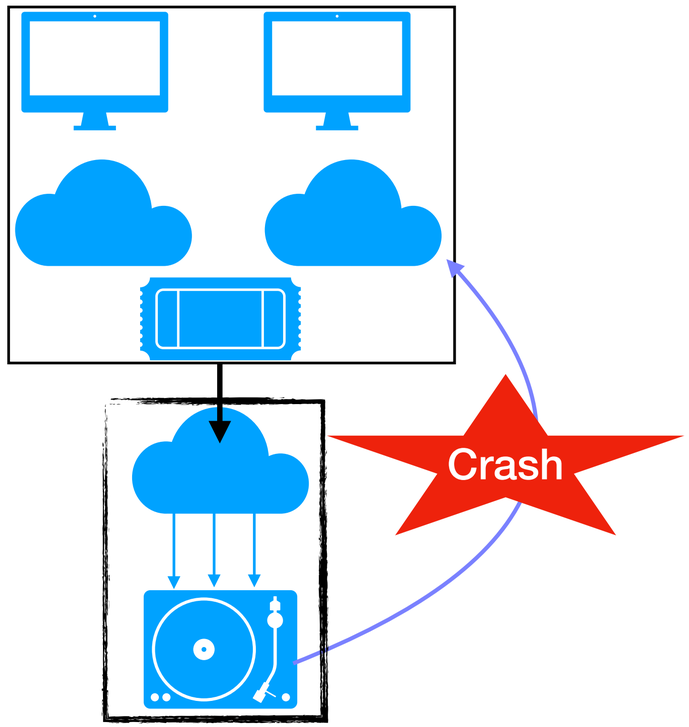
Concurrent Memory Systems + Persistency



Persistency

- Archives writes, not necessarily in order
- Re-orders incoming writes
- Fences can impose ordering

Concurrent Memory Systems + Persistency



Persistency

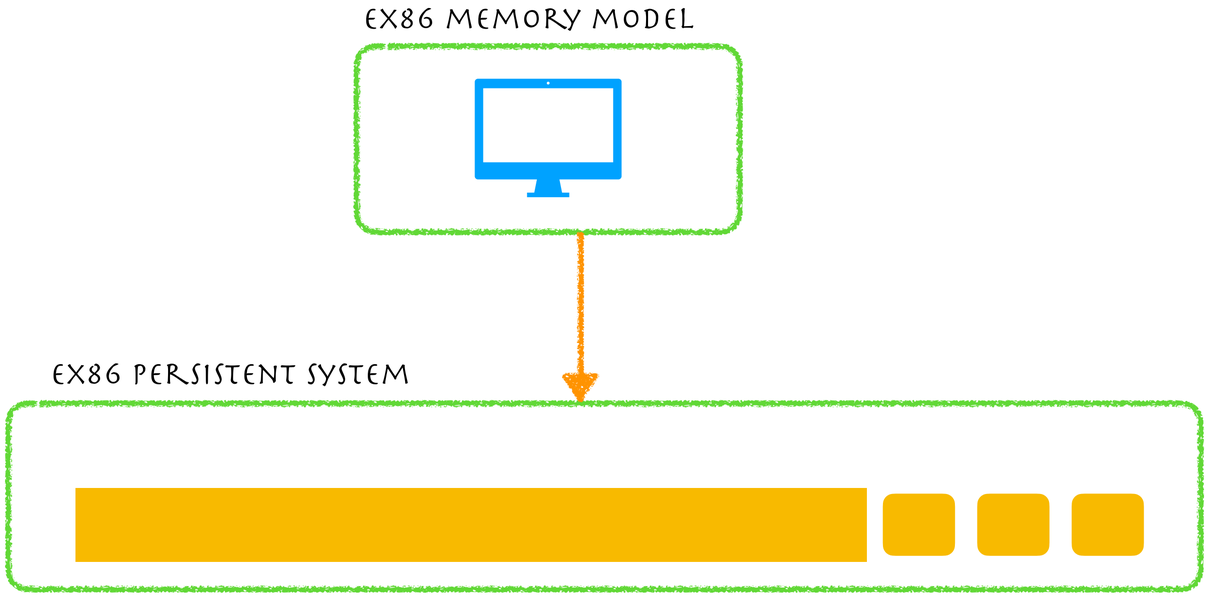
Archives writes, not necessarily in order

Re-orders incoming writes

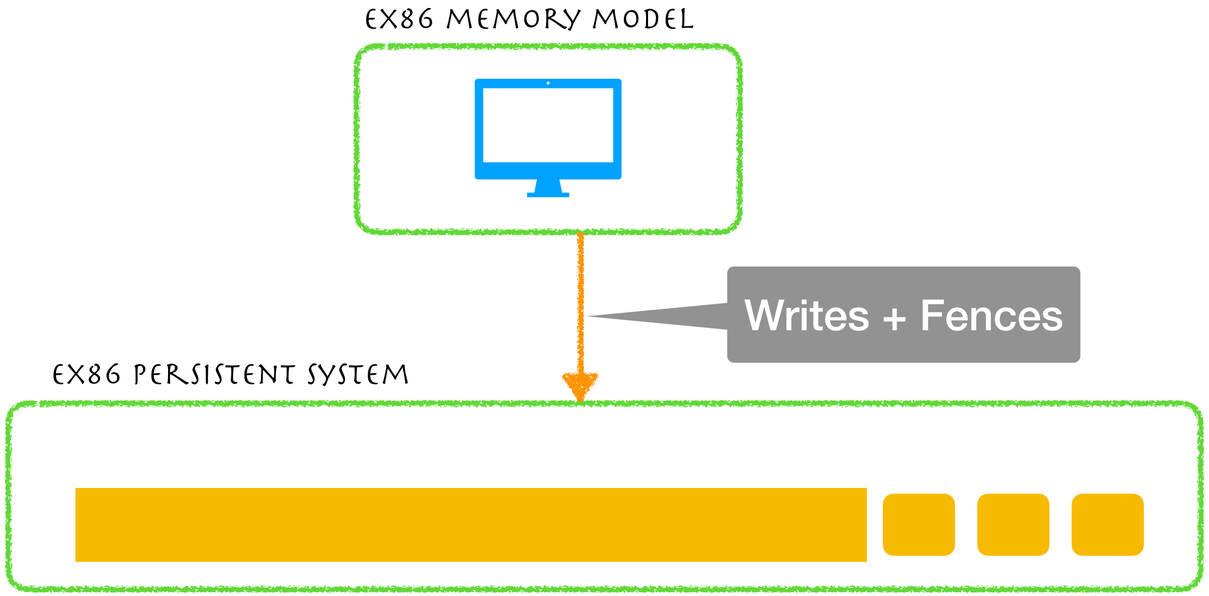
Fences can impose ordering

Useful in case of a crash

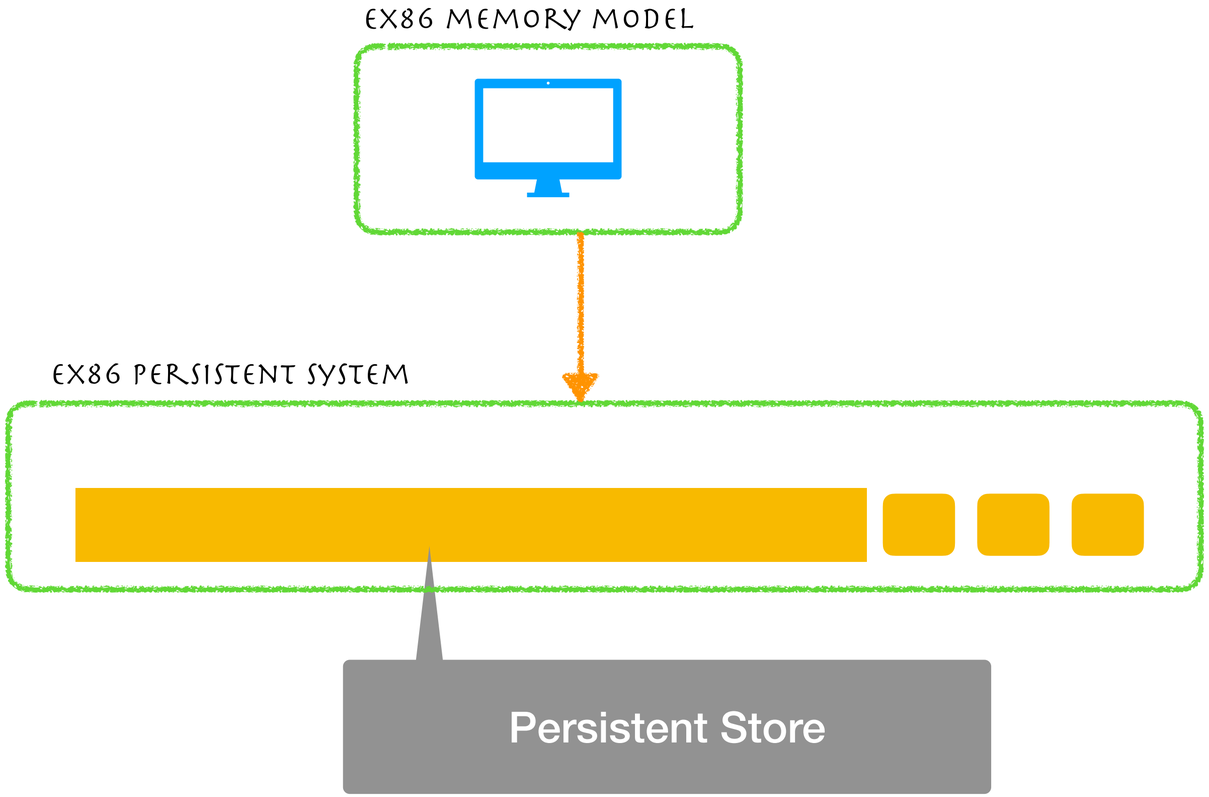
Extended x86 Persistent System



Extended x86 Persistent System



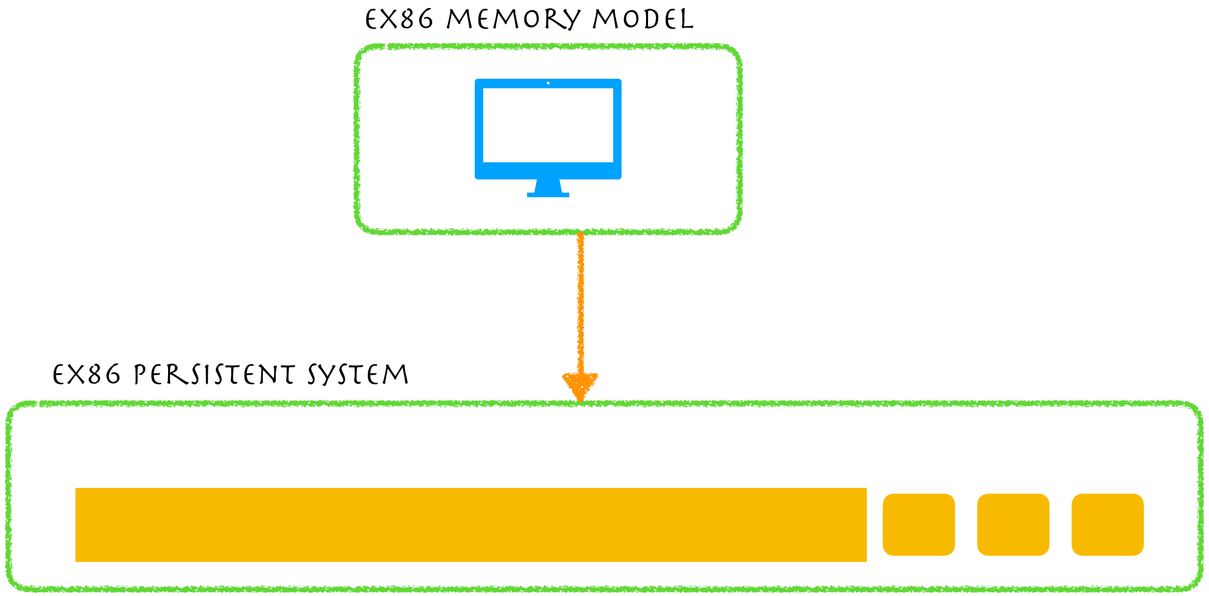
Extended x86 Persistent System



Extended x86 Persistent System

Instructions

Wb(x,d) ntw(x,d) Fl(x) Sf Fo(x)



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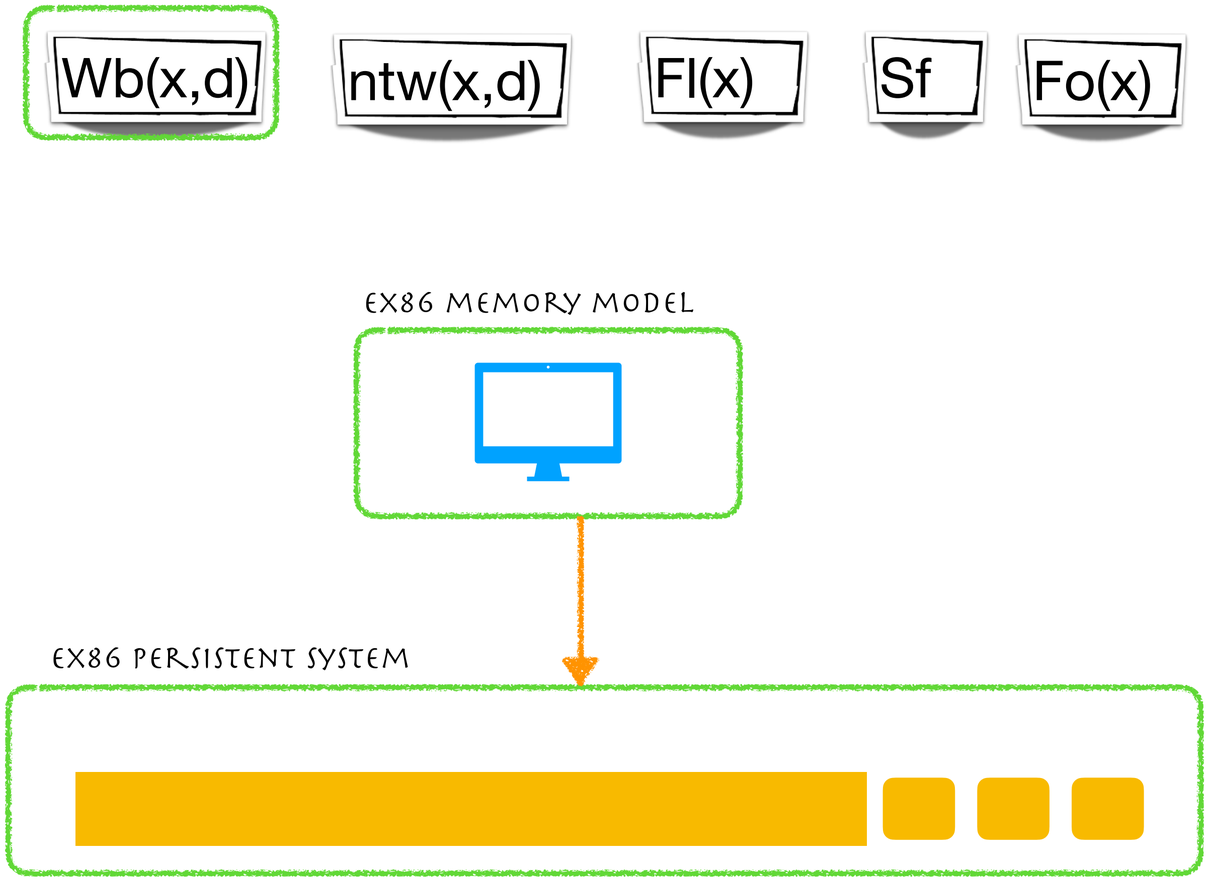

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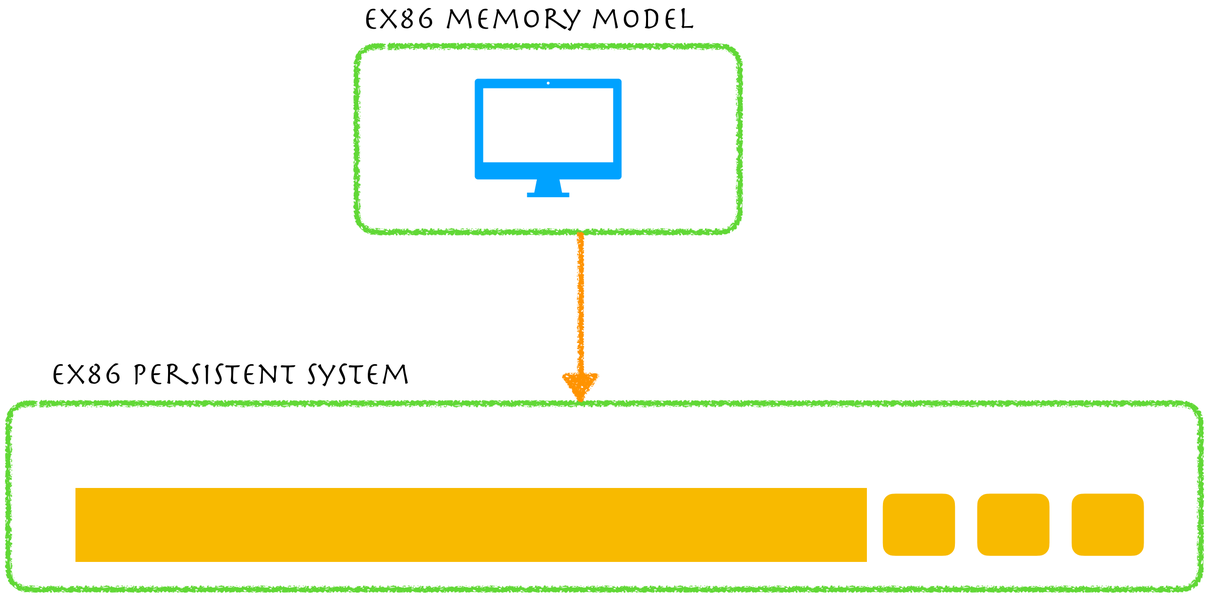
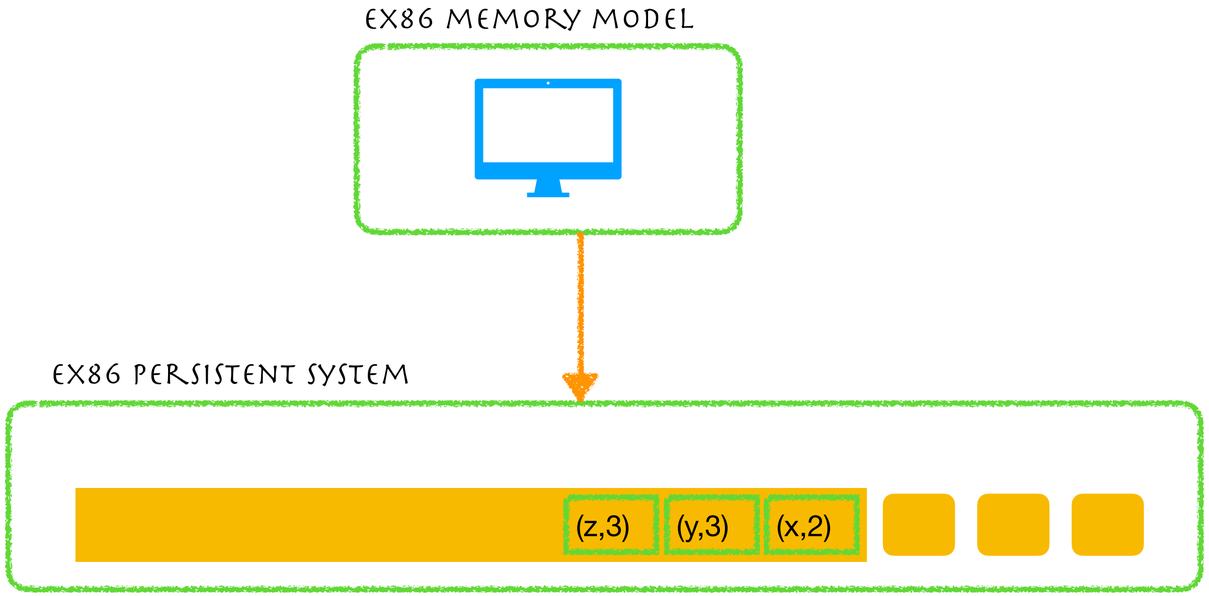


Wb writes are buffered

Extended x86 Persistent System

Instructions

Wb(x,d) ntw(x,d) Fl(x) Sf Fo(x)



Wb writes are buffered

Extended x86 Persistent System

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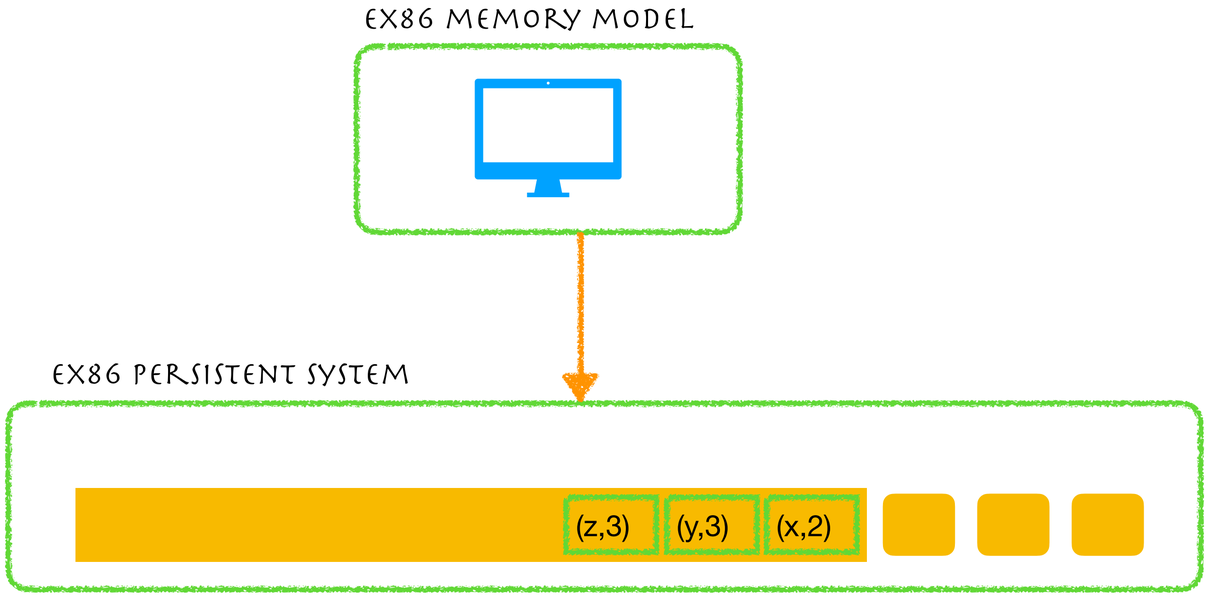


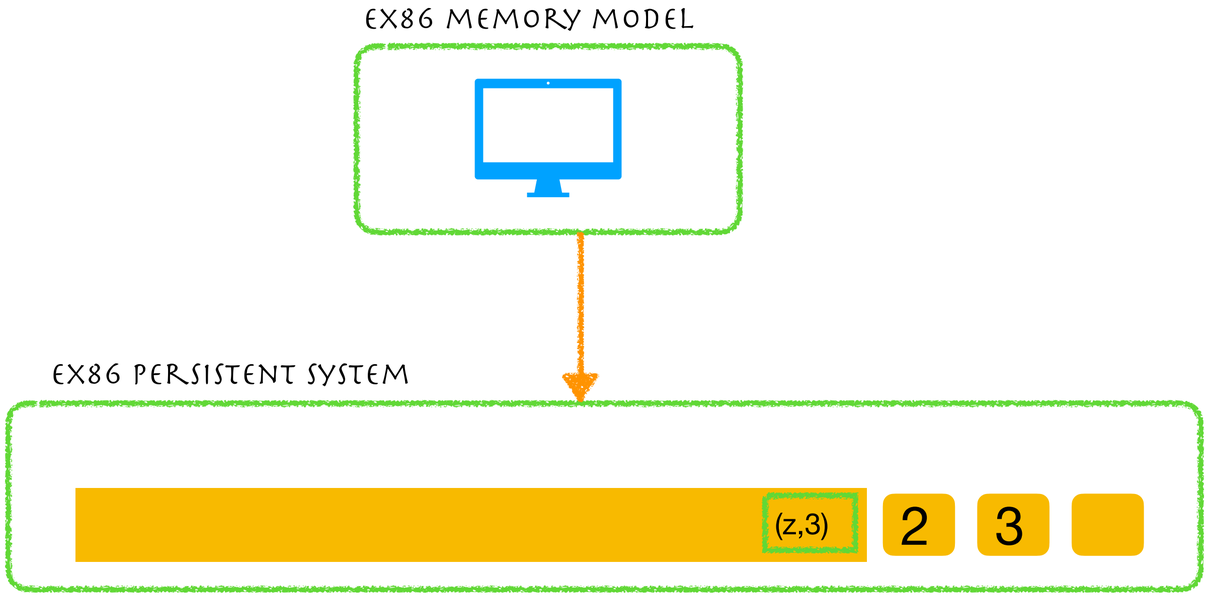
Propagated non-deterministically

Only per variable ordering

Extended x86 Persistent System

Instructions

Wb(x,d) ntw(x,d) Fl(x) Sf Fo(x)



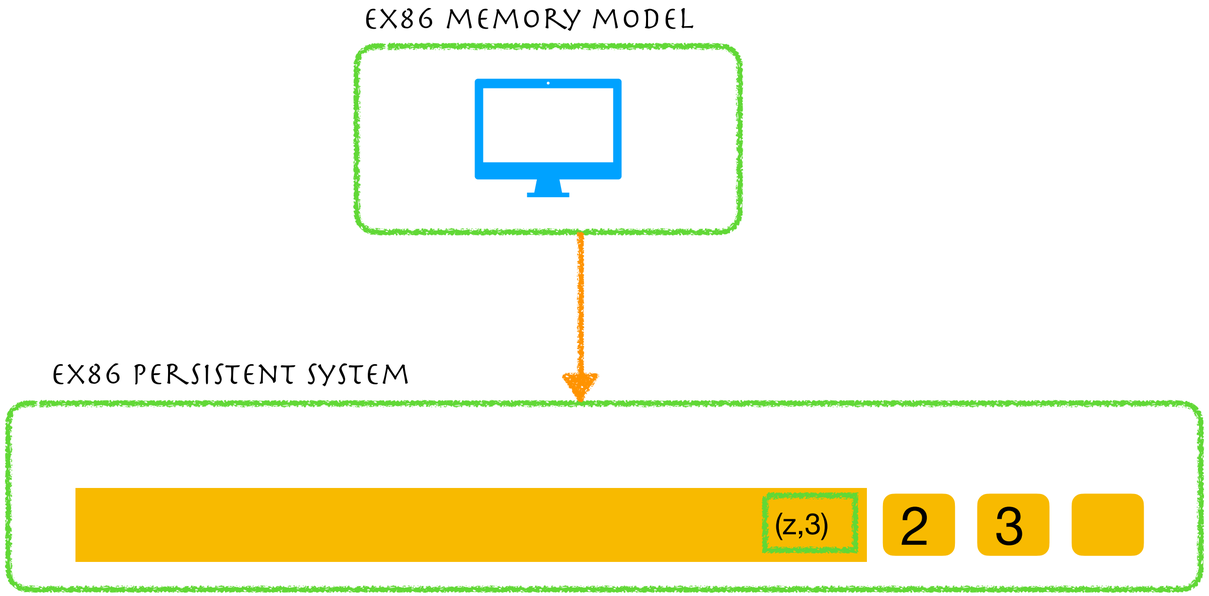
Propagated non-deterministically

Only per variable ordering

Extended x86 Persistent System

Instructions

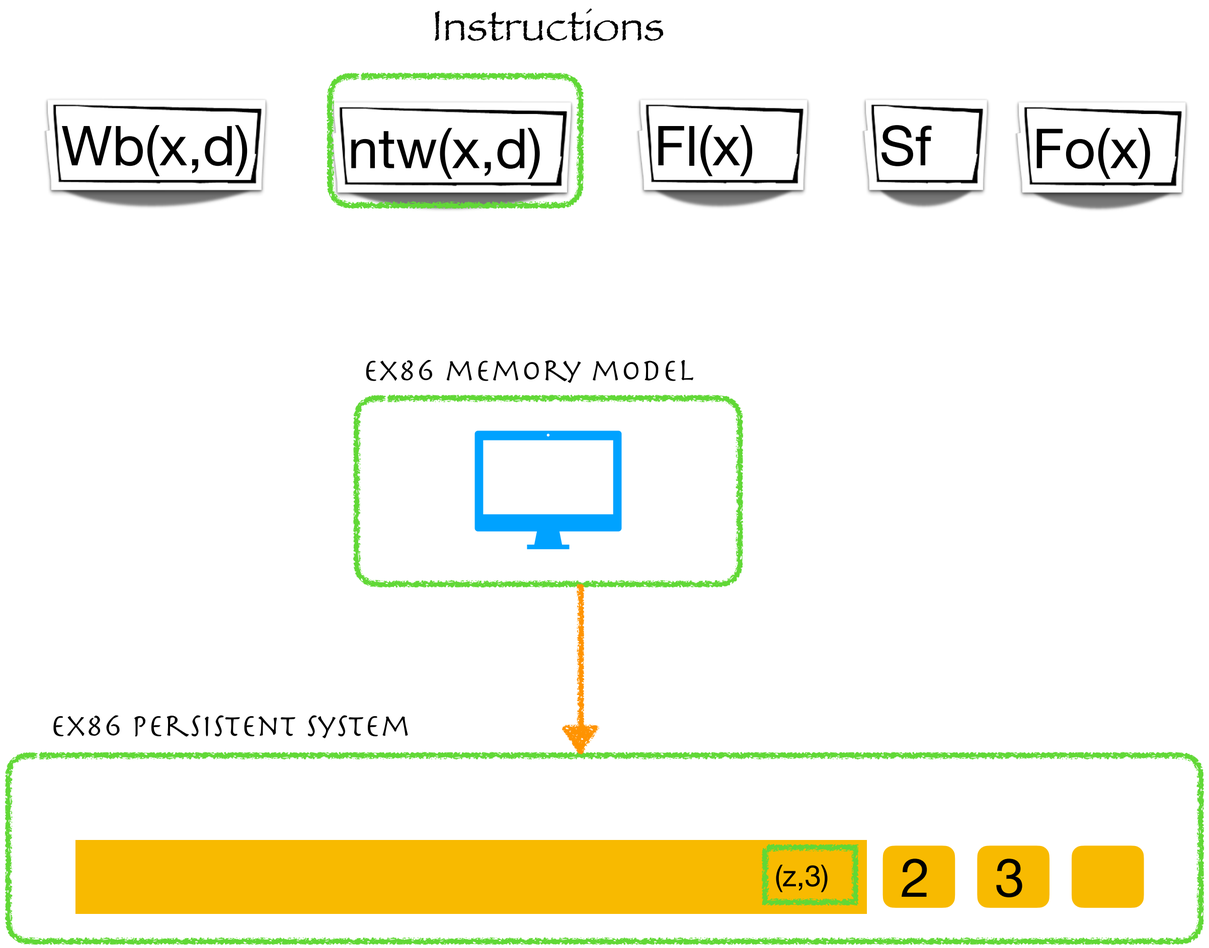
Wb(x,d) | ntw(x,d) | Fl(x) | Sf | Fo(x)



Propagated non-deterministically

Only per variable ordering

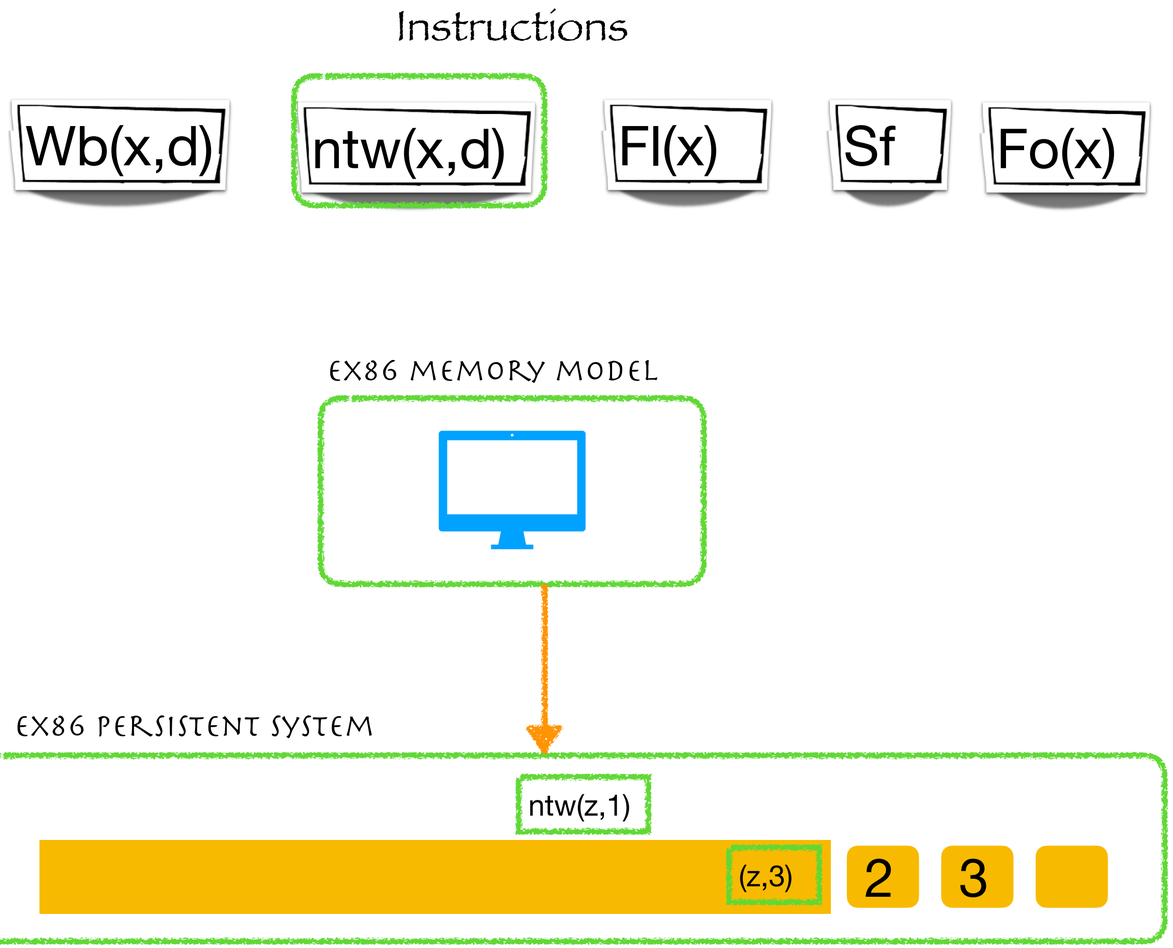
Extended x86 Persistent System



Ntw writes are propagated directly

Ensures no pending writes on the variable

Extended x86 Persistent System



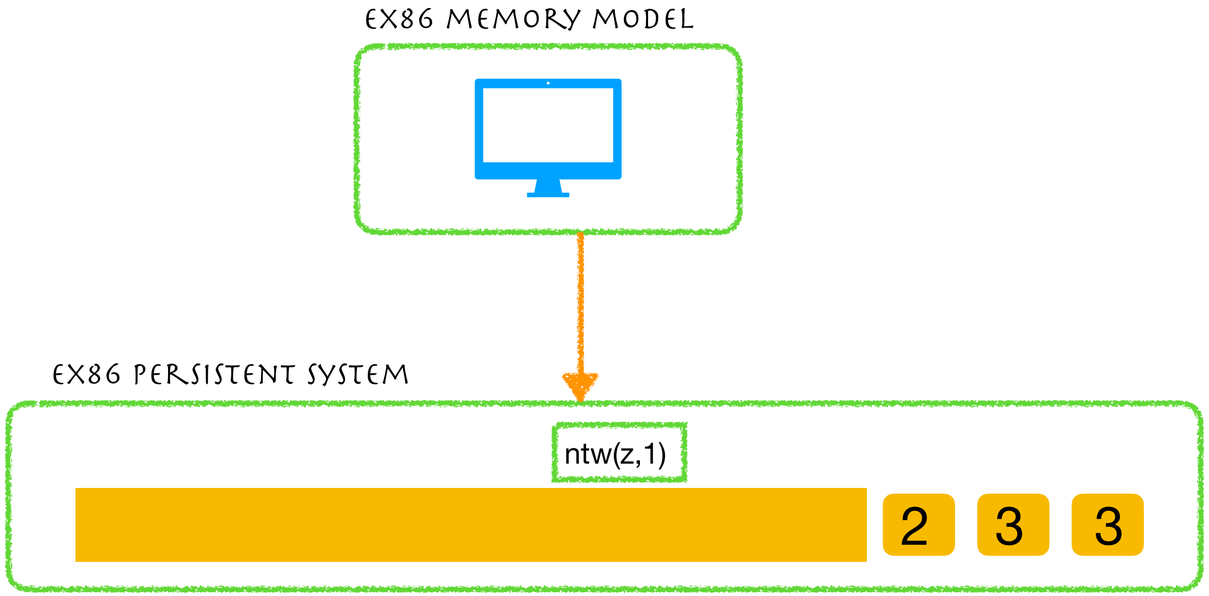
Ntw writes are propagated directly

Ensures no pending writes on the variable

Extended x86 Persistent System

Instructions

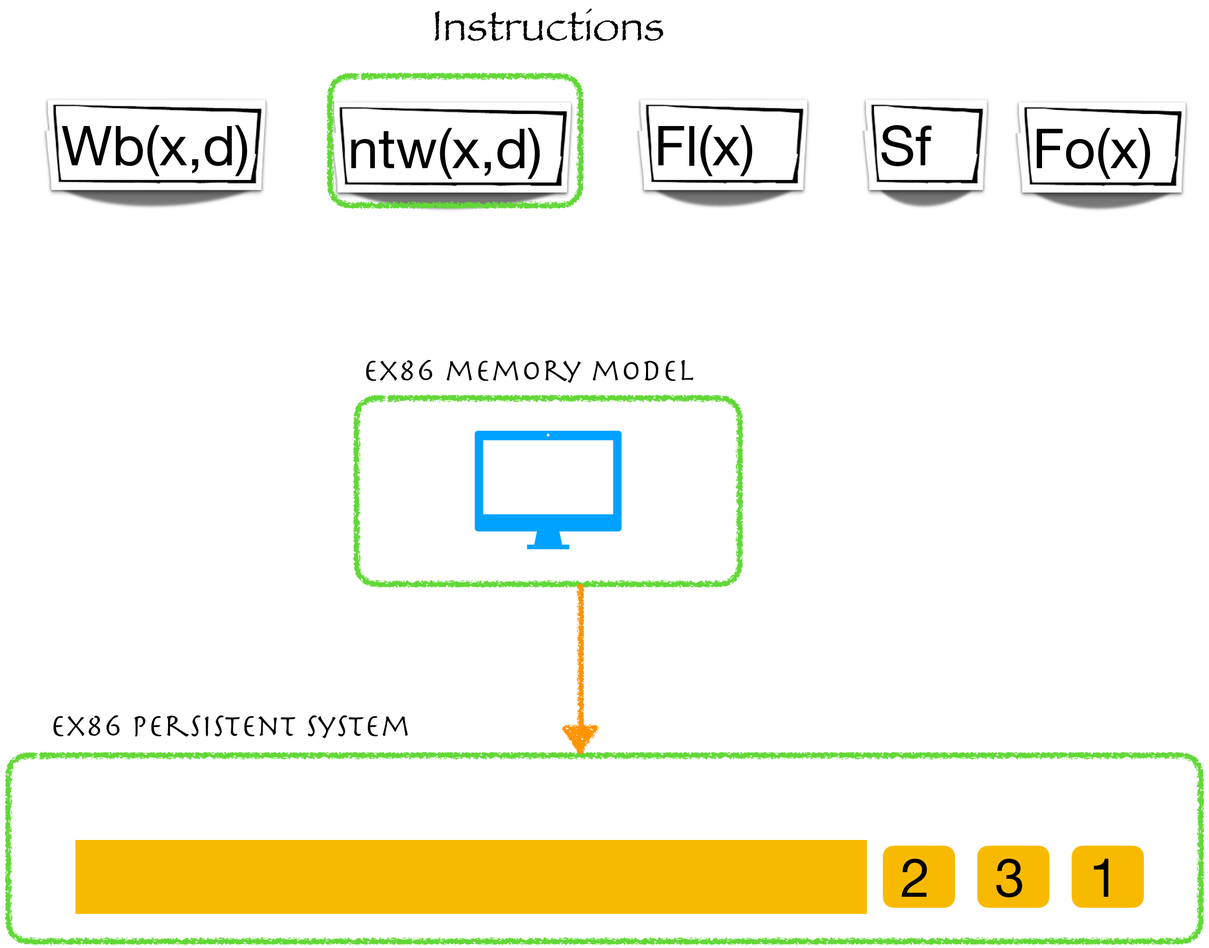
Wb(x,d) | ntw(x,d) | Fl(x) | Sf | Fo(x)



Ntw writes are propagated directly

Ensures no pending writes on the variable

Extended x86 Persistent System



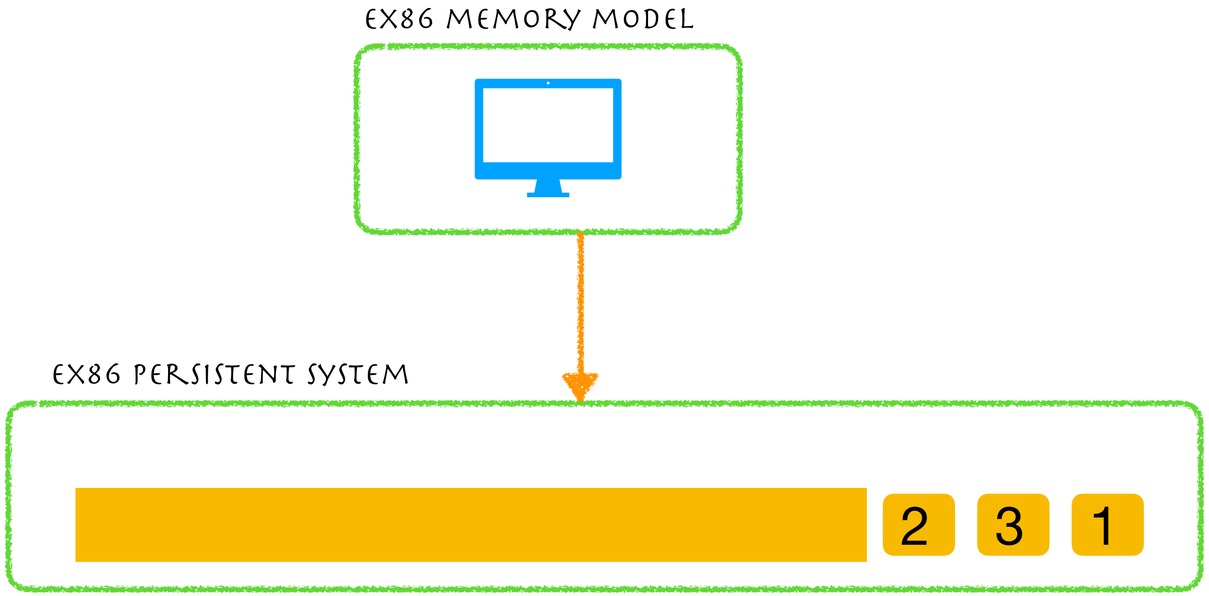
Ntw writes are propagated directly

Ensures no pending writes on the variable

Extended x86 Persistent System

Instructions

Wb(x,d) ntw(x,d) Fl(x) Sf Fo(x)



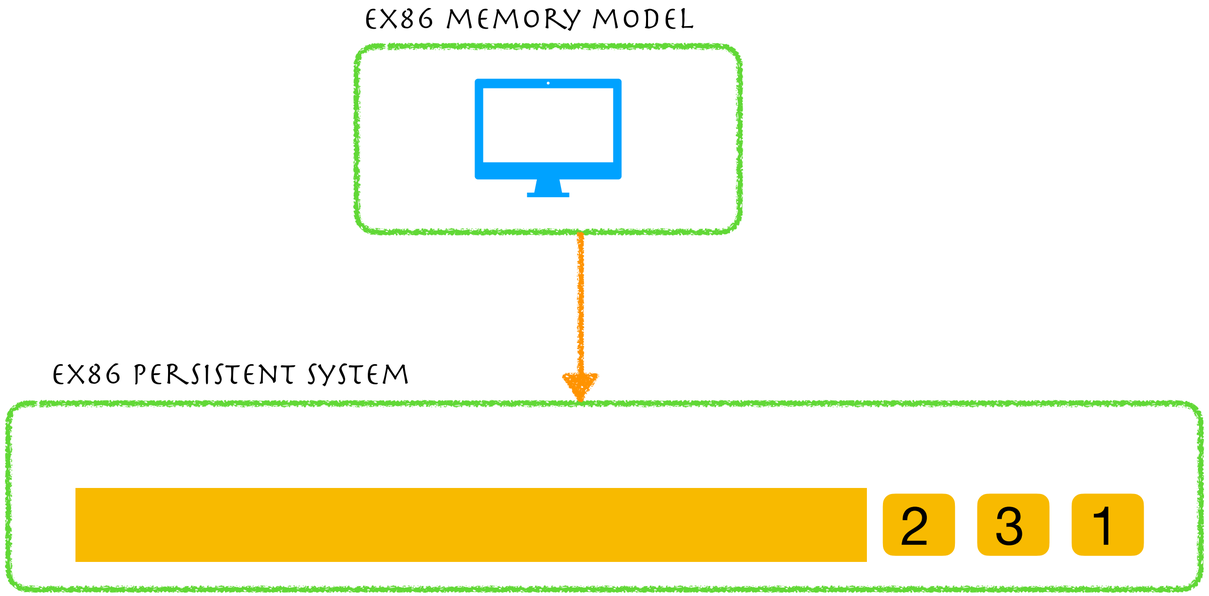
Ntw writes are propagated directly

Ensures no pending writes on the variable

Extended x86 Persistent System

Instructions

Wb(x,d) ntw(x,d) Fl(x) Sf Fo(x)

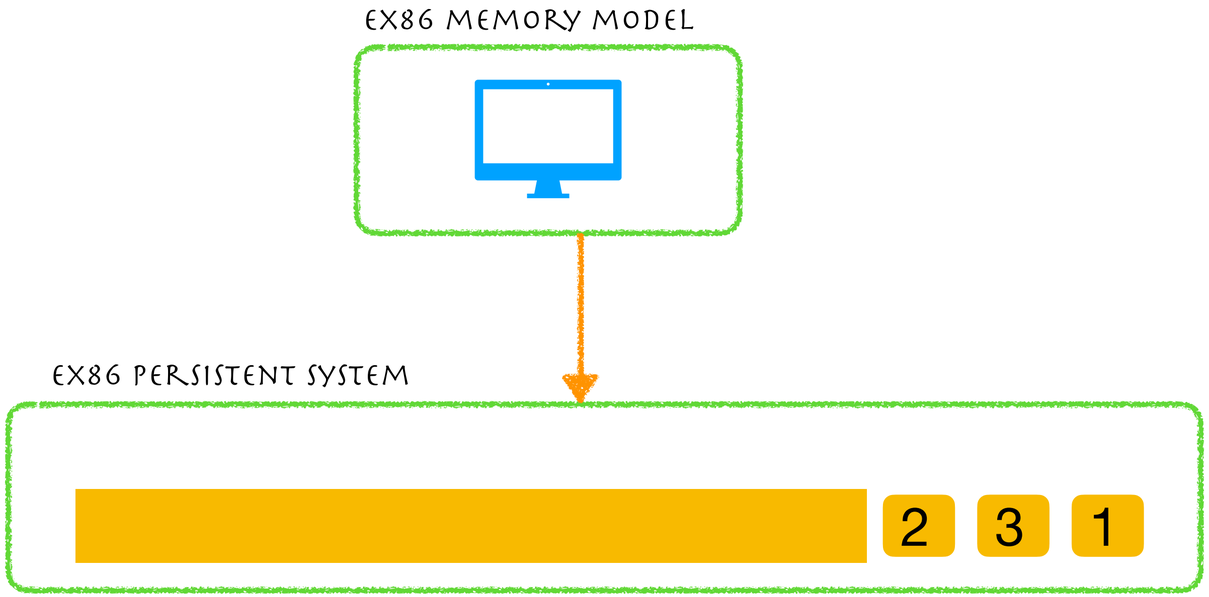


Fl ensures no pending writes on the variable

Extended x86 Persistent System

Instructions

Wb(x,d) ntw(x,d) Fl(x) Sf Fo(x)

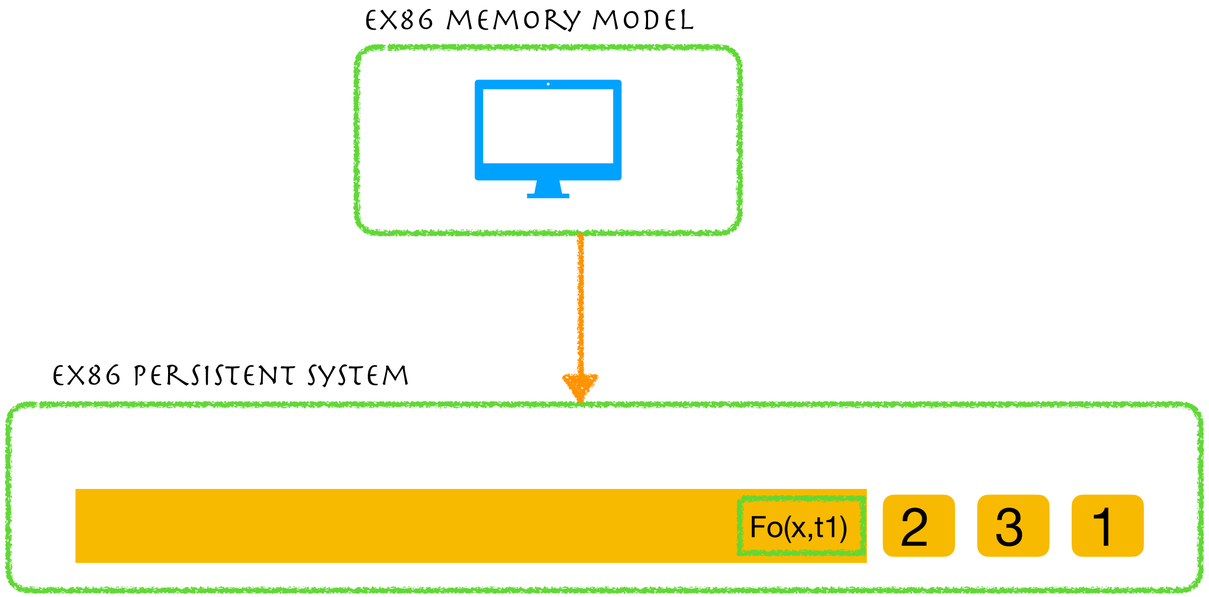


Fl ensures no pending writes on the variable

Extended x86 Persistent System

Instructions

Wb(x,d) ntw(x,d) Fl(x) Sf Fo(x)



Fo is buffered with thread information

SF ensures no pending Fo of that thread

Extended x86 Persistent System

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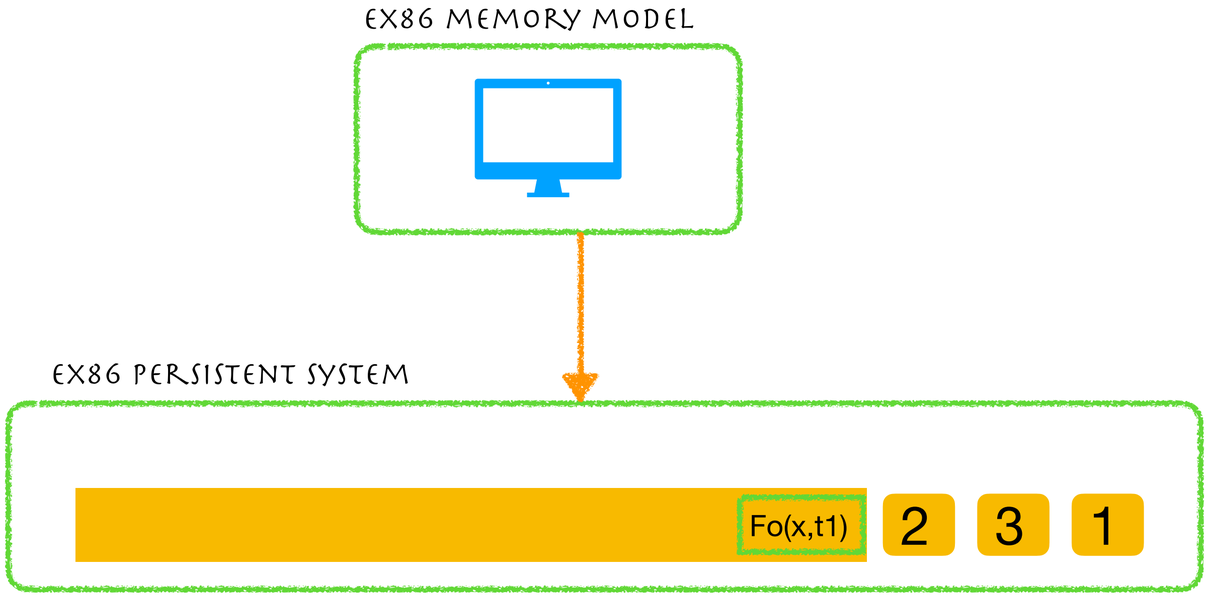


Fo is buffered with thread information

SF ensures no pending Fo of that thread

Ensures prior writes by the thread are persisted

VERIFICATION

Crisis and deadlocks when they occur have at least this advantage.: they force us to think

Verifying Concurrent Systems

Verifying Concurrent Systems

Verifying Concurrent Systems

Correctness
Specification

Verifying Concurrent Systems

$\models$

Correctness Specification

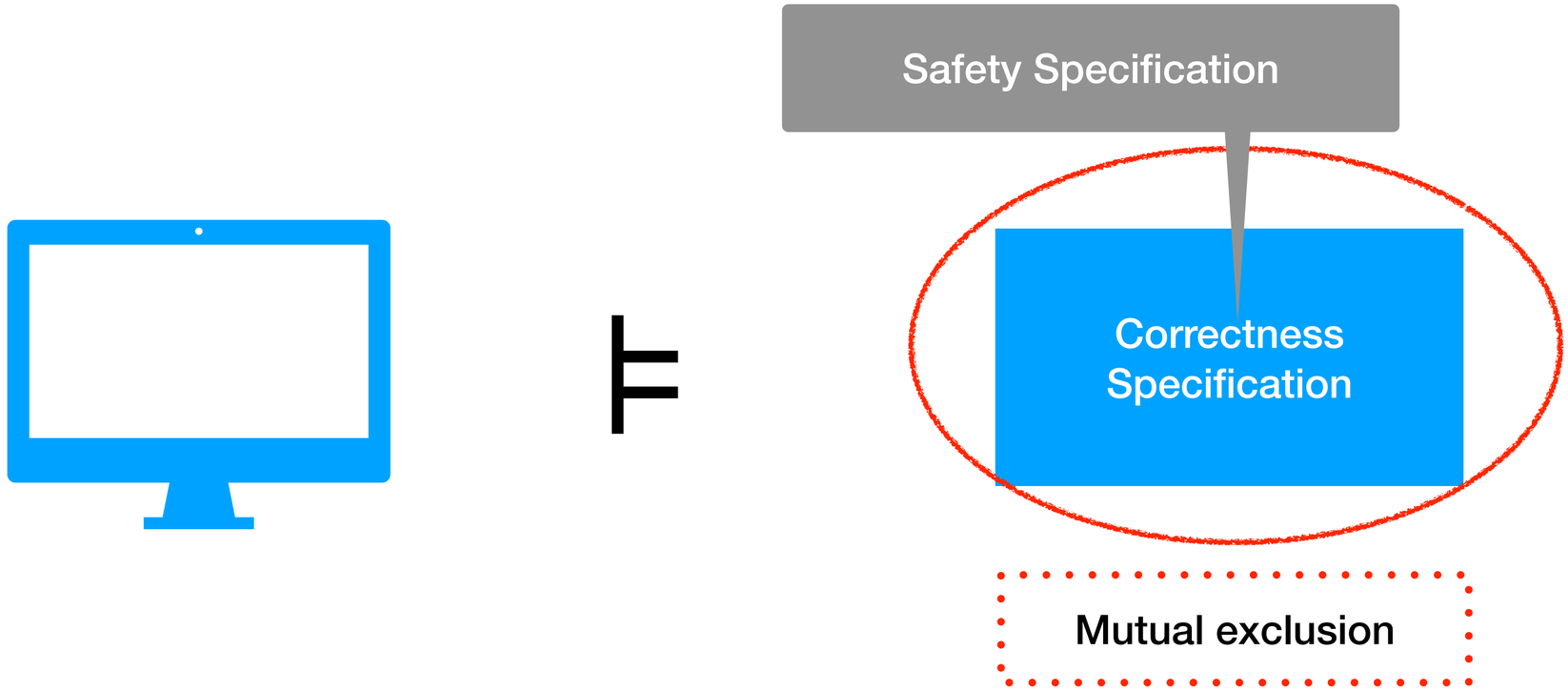
Verifying Concurrent Systems

$\models$

Correctness Specification

Mutual exclusion

Verifying Concurrent Systems



Verifying Concurrent Systems

$\models$

Correctness Specification

Mutual exclusion

Sequential Consistency	PSPACE-Complete
TSO	Non-primitive recursive
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Verifying Concurrent Systems

$\models$

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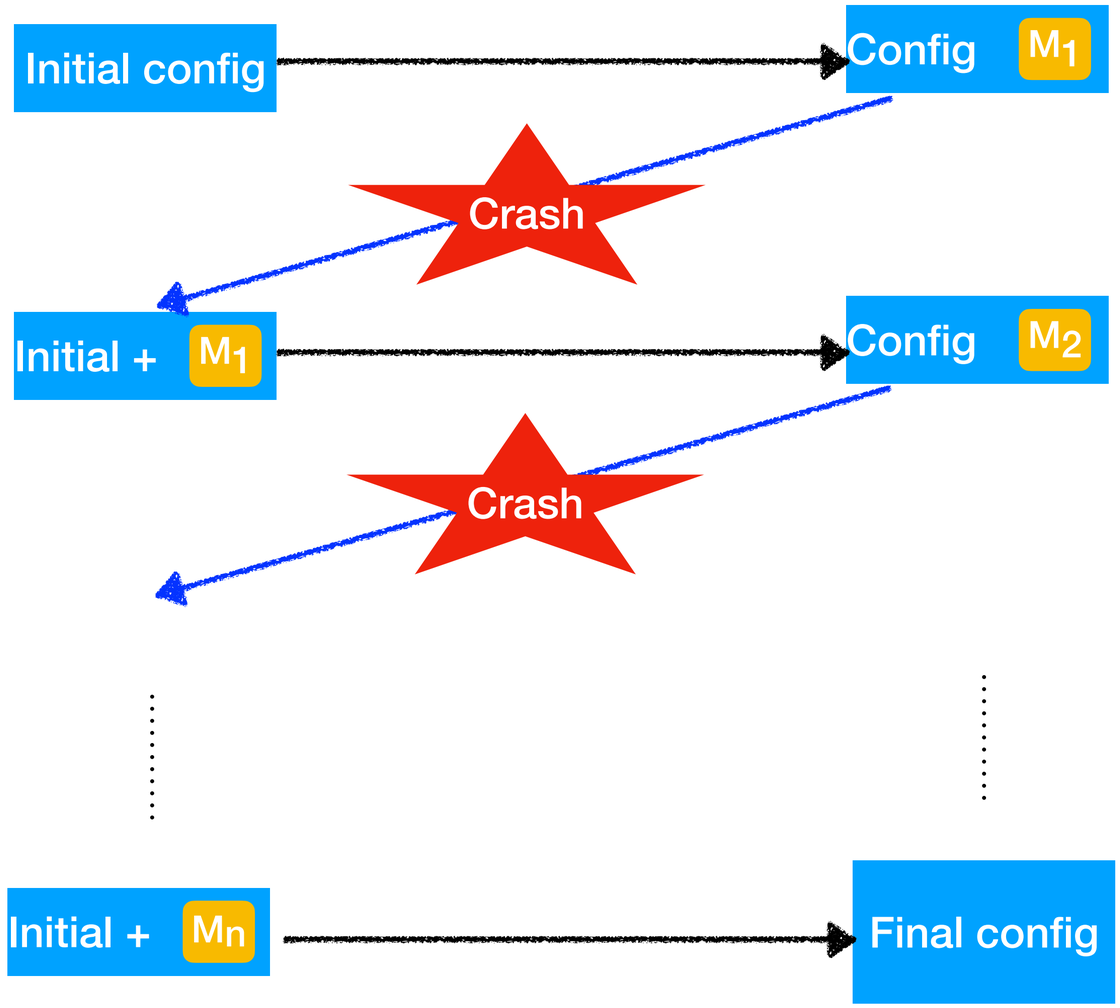
Theory of Well Structured Transition Systems

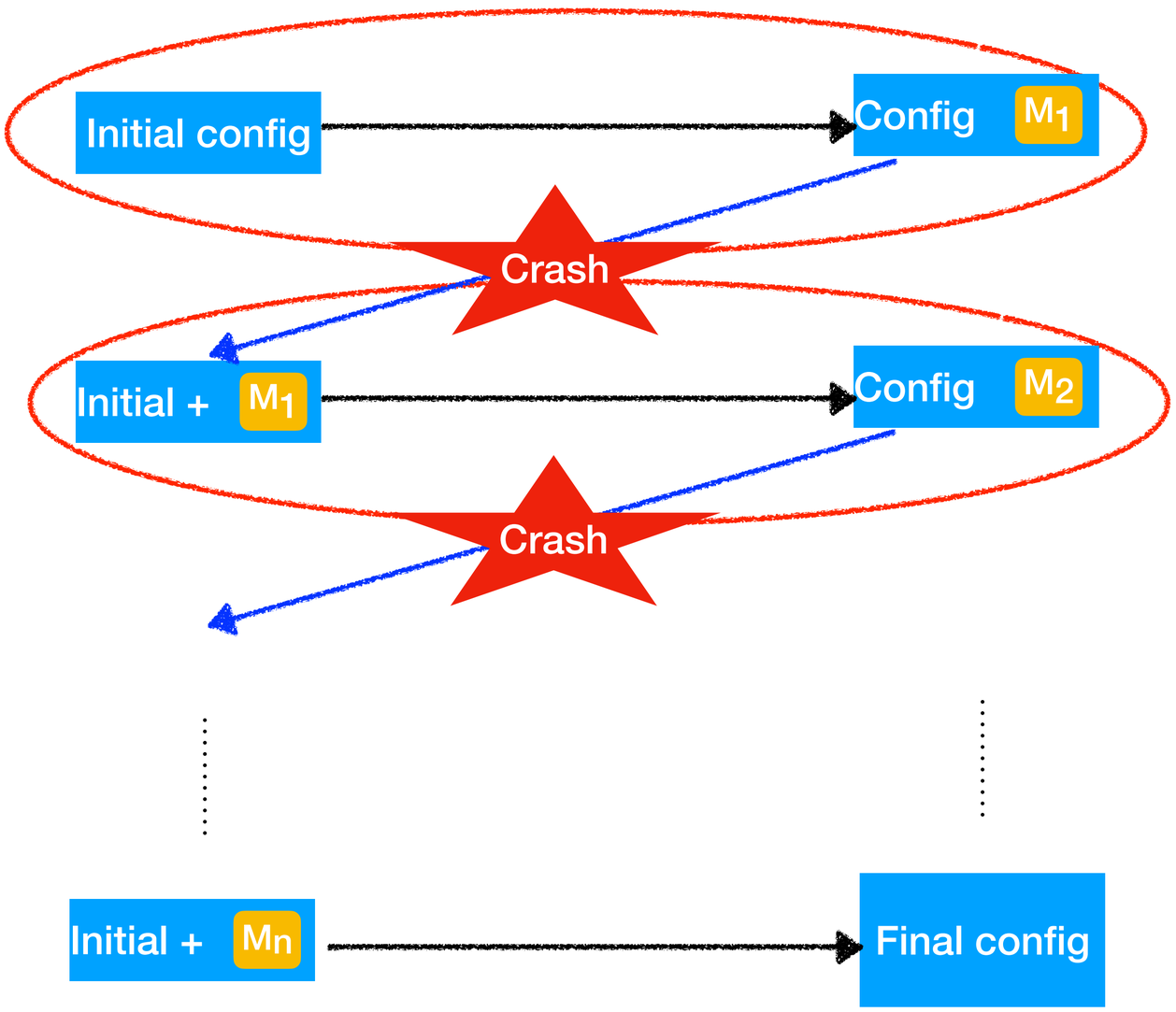
Persistent Reachability Problem

Persistent Reachability Problem



Persistent reachability: Whether programs can reach a program location in presence of crashes

Persistent Reachability Problem

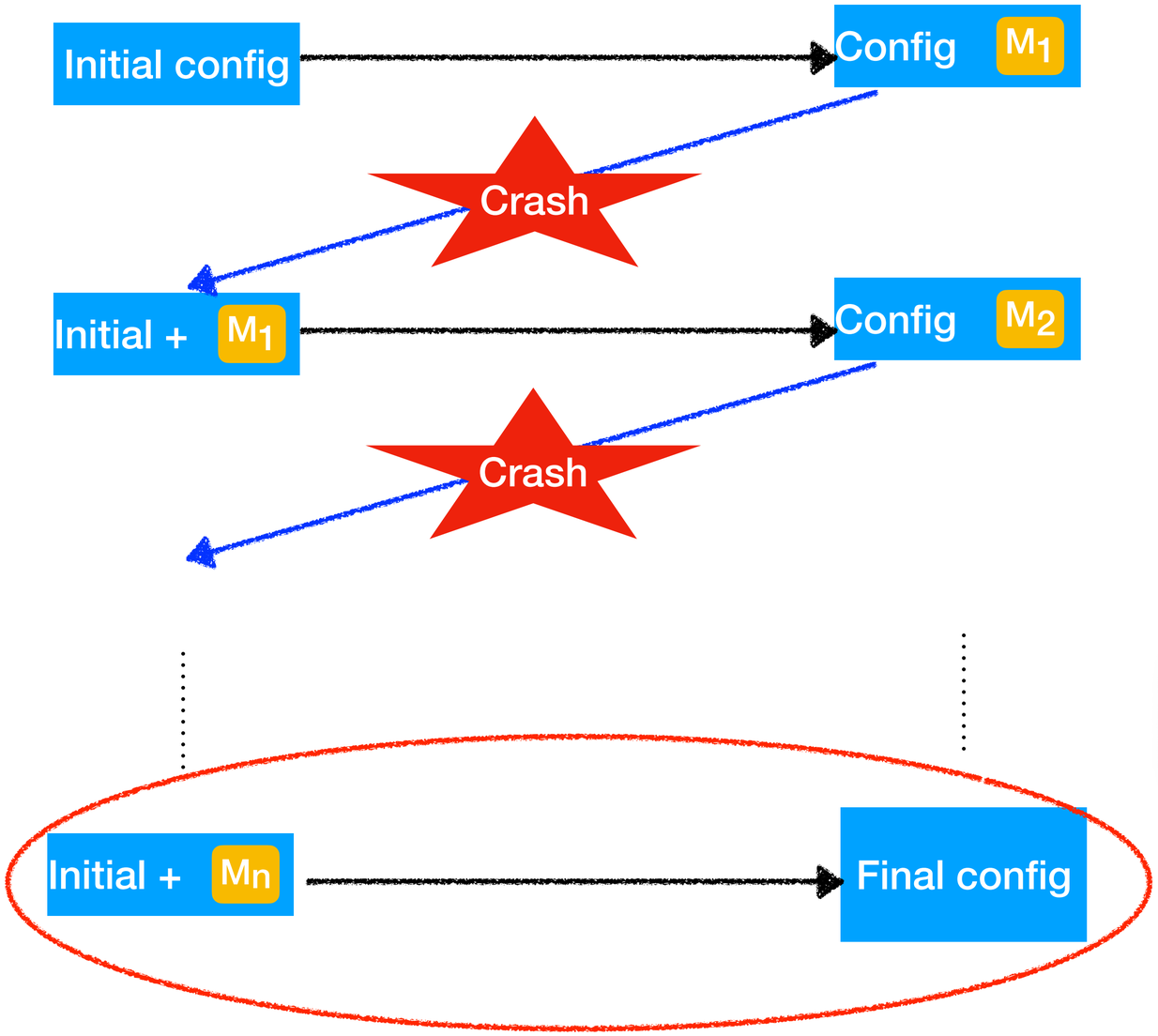


Persistent reachability: Whether programs can reach a program location in presence of crashes

Persistent memory

Whether a persistent memory can be reached

Persistent Reachability Problem



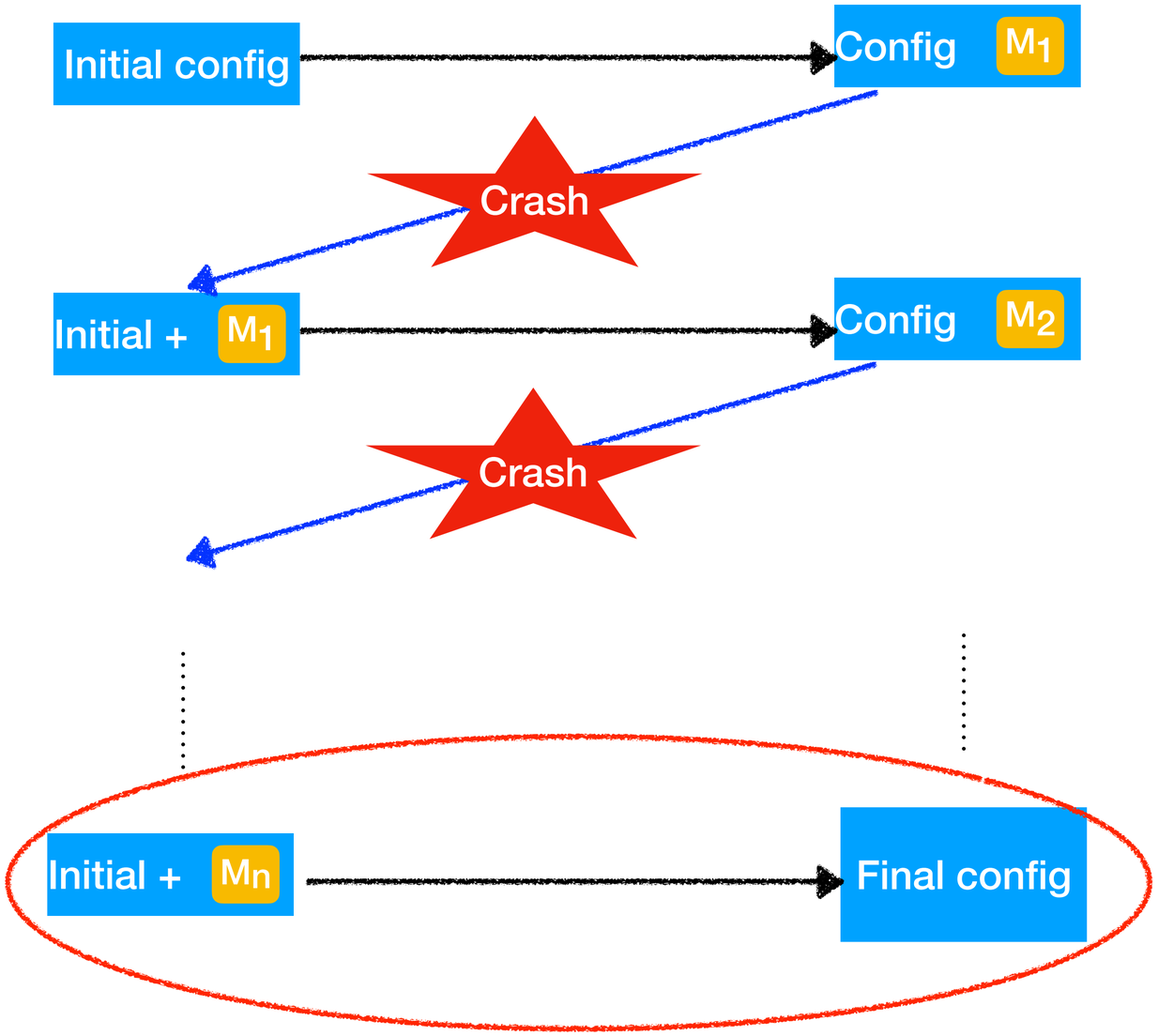
Persistent reachability: Whether programs can reach a program location in presence of crashes

Crash free reachability

Persistent memory

State reachability without crashes

Persistent Reachability Problem



Persistent reachability: Whether programs can reach a program location in presence of crashes

Crash free reachability + Persistent memory

VERIFYING EX86 WITH PERSISTENCY

All stable processes we shall predict. all unstable processes we shall control - John Von Neumann

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Verification under Intel-x86 with Persistency

PAROSH ABDULLA, Uppsala University, Sweden
MOHAMED FAOUZI ATIG, Uppsala University, Sweden
AHMED BOUAJJANI, Université Paris Cité, France
K. NARAYAN KUMAR, Chennai Mathematical Institute and IRL ReLaX, India
PRAKASH SAIVASAN, Institute of Mathematical Sciences, HBNI and IRL ReLaX, India

Persistent Memory Reachability

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Persistent reachability problem reduces to crash free reachability in a new program

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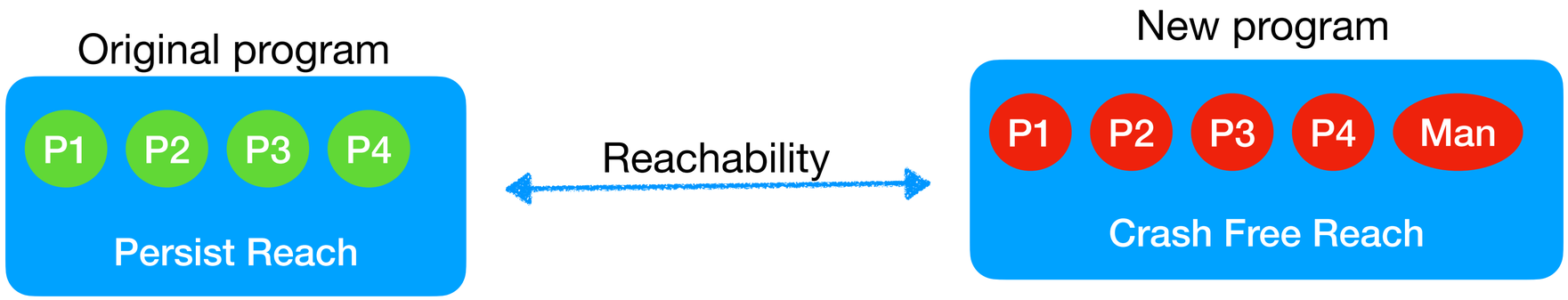

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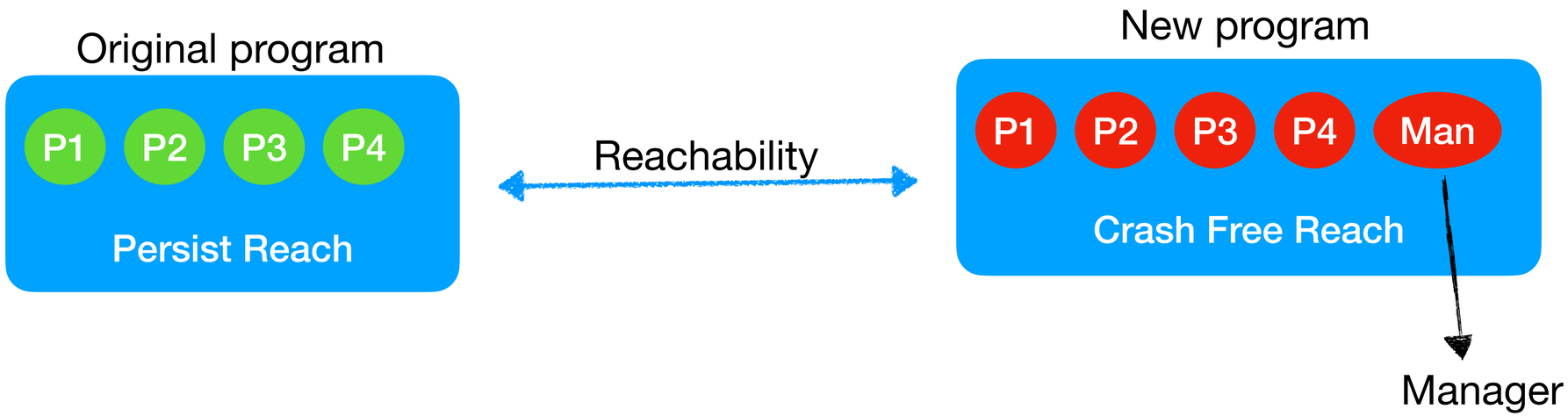

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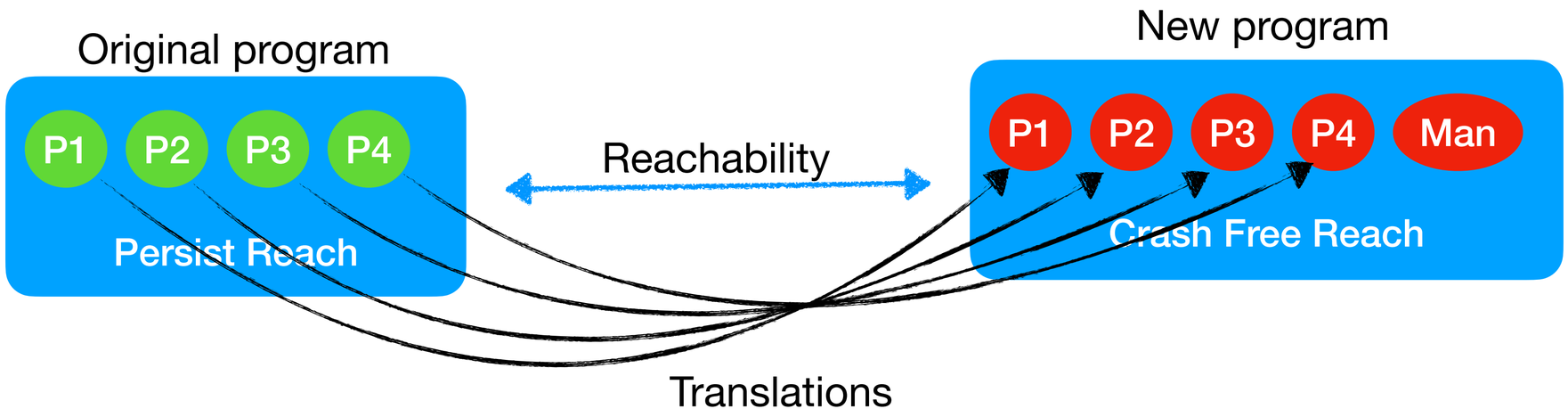

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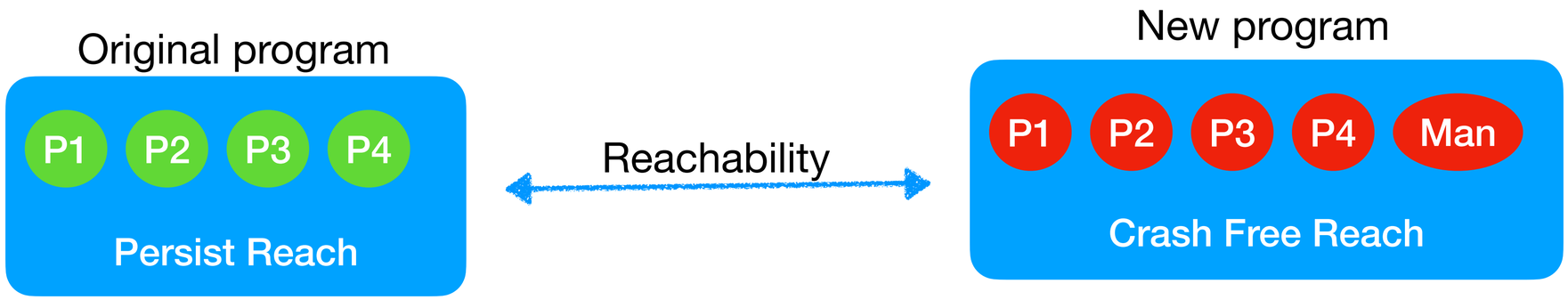

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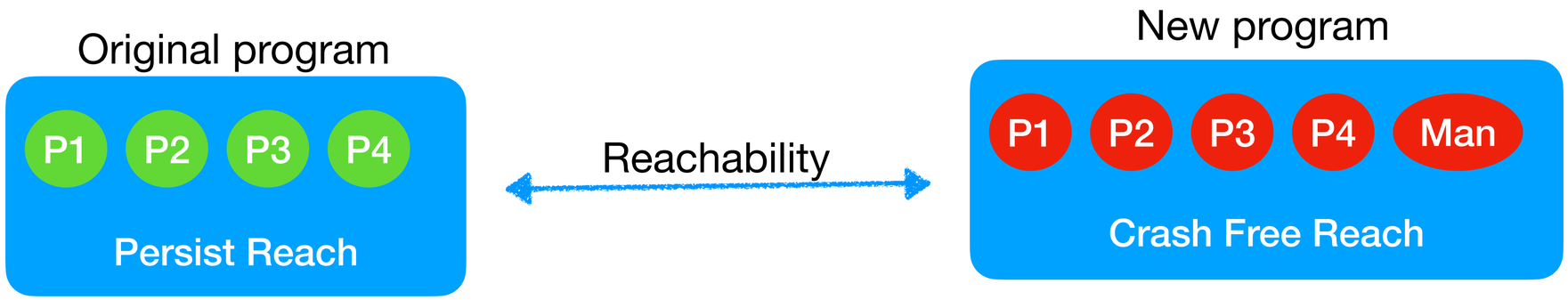

Translation employs a guess and verify technique

Persistent Memory Reachability

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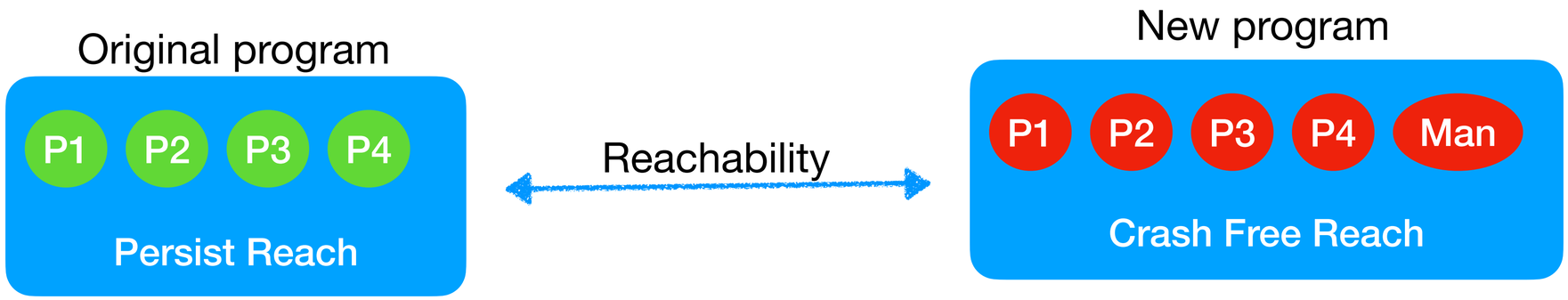

Translation employs a guess and verify technique

Guess the writes that will persist last

Persistent Memory Reachability

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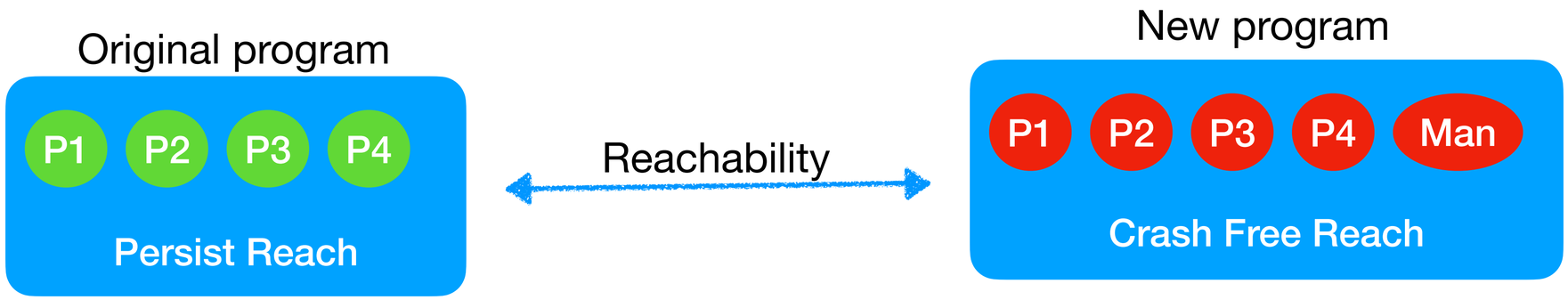
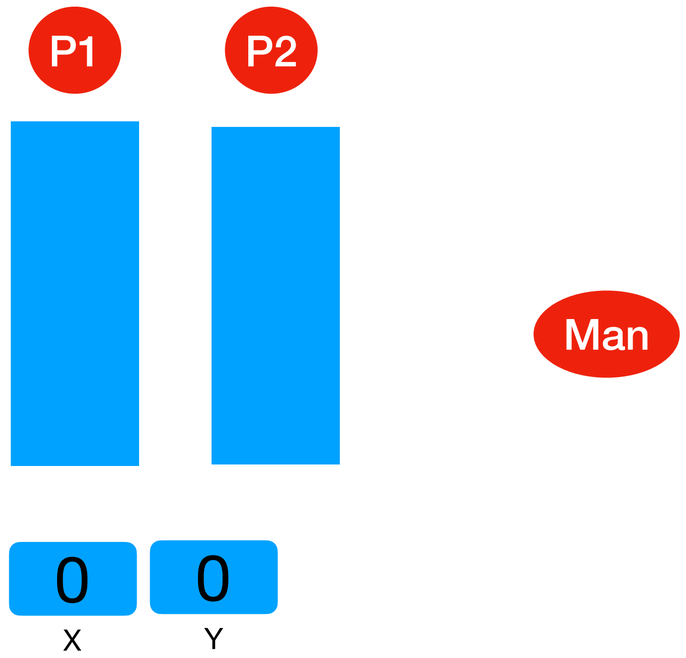


Translation employs a guess and verify technique

Ensure that the guessed writes are not overwritten

Persistent Memory Reachability



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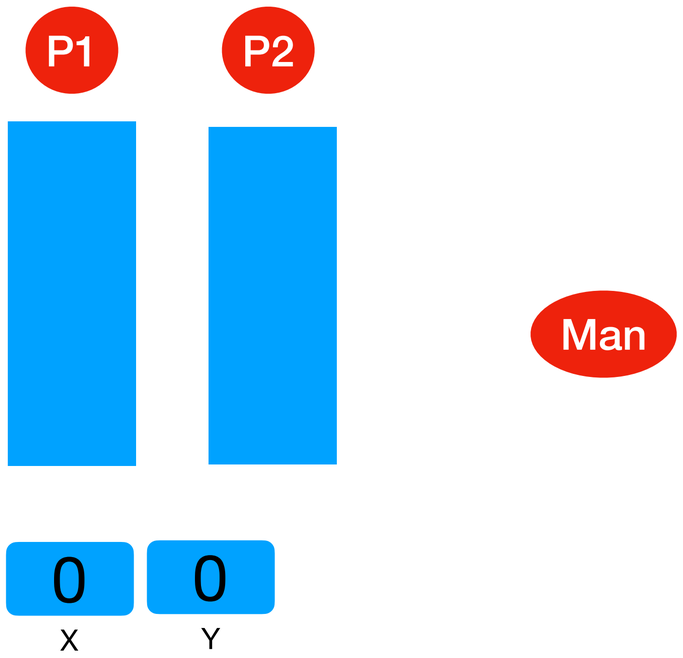
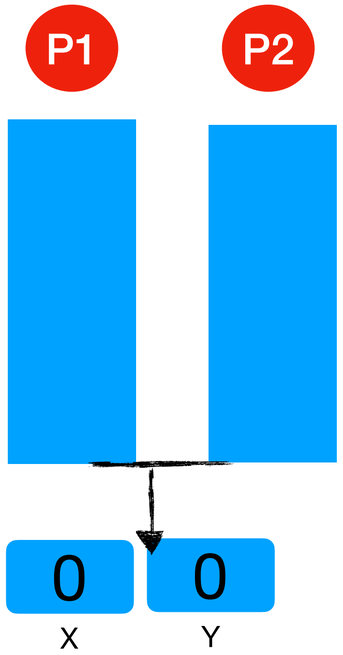


Man

Idea involves the manager speculating a write that will persist

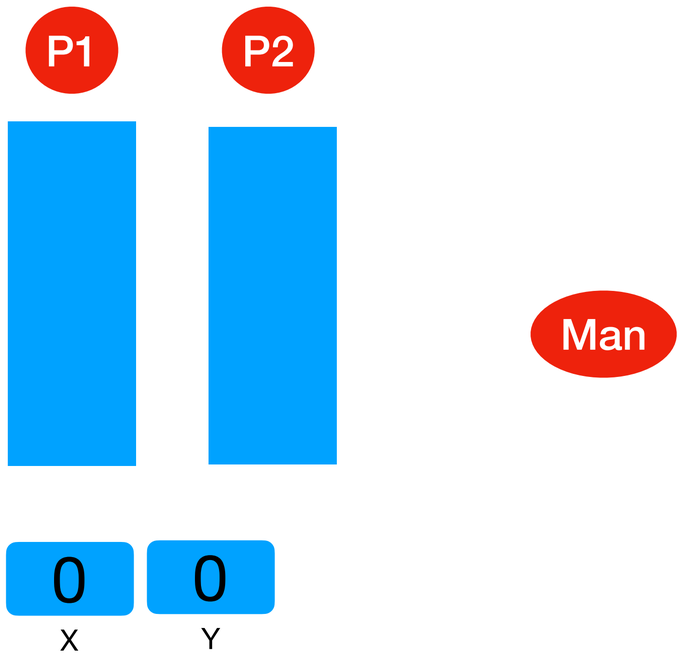
Persistent Memory Reachability



Man

Manager cannot observe all writes

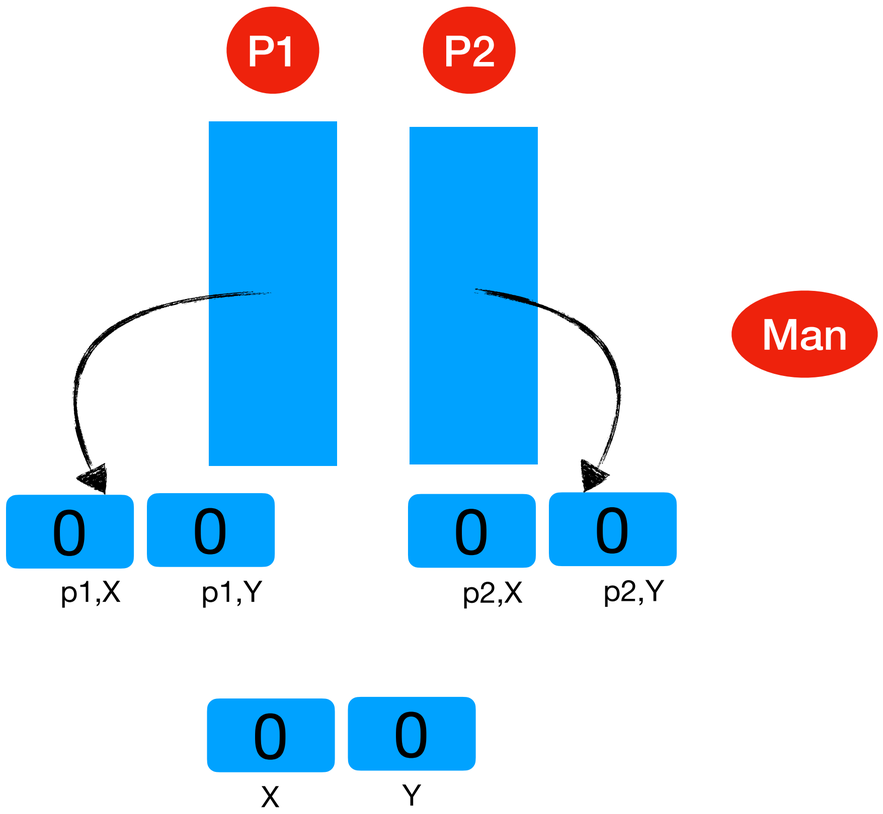
Persistent Memory Reachability



Man

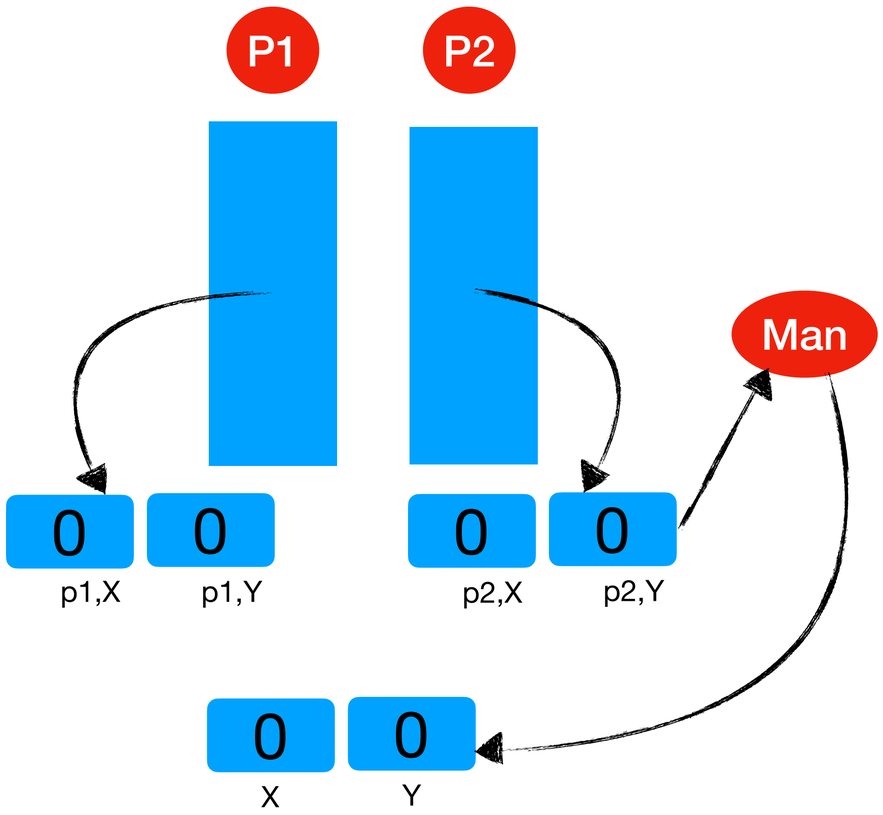
Introduce per process memory

Persistent Memory Reachability



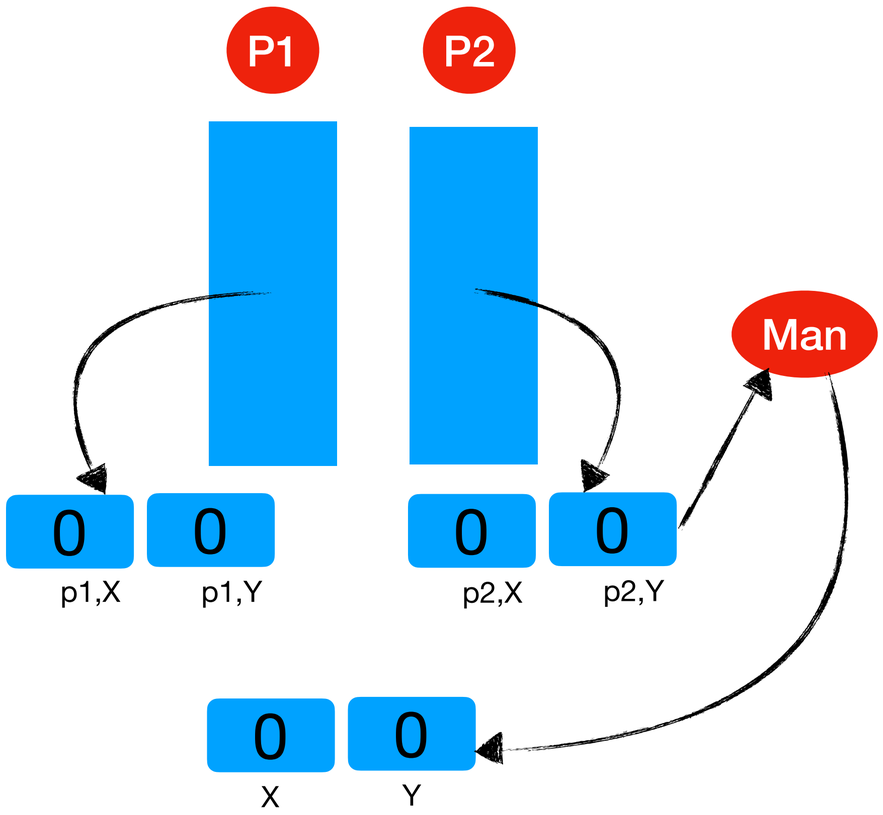
Threads write to their copy

Persistent Memory Reachability



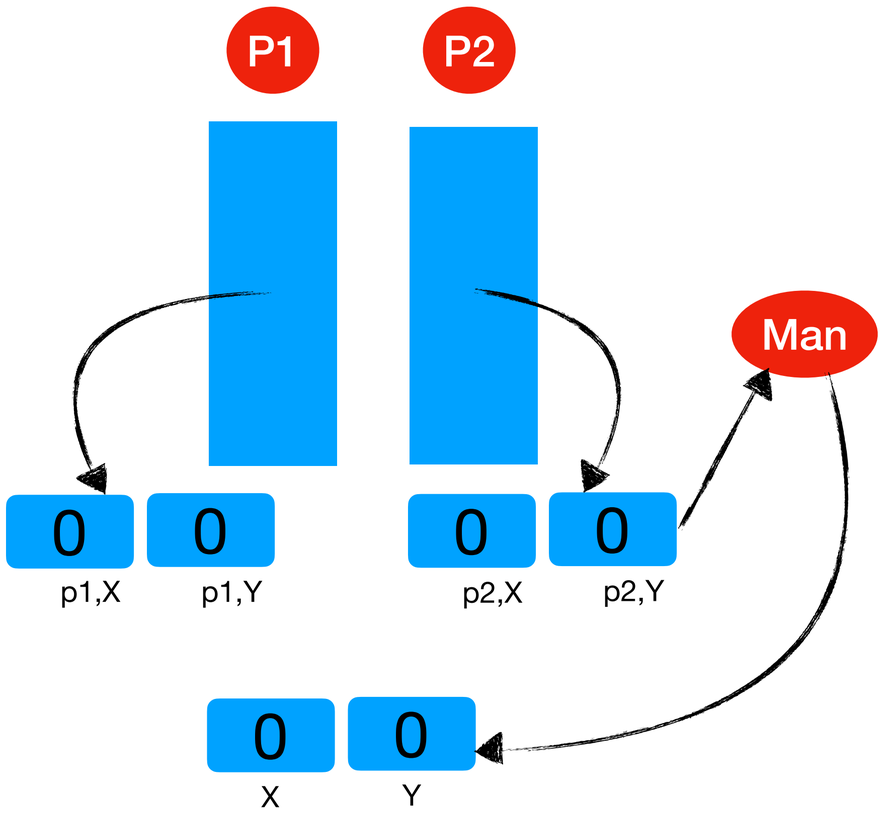
Manager transfers to the main memory

Persistent Memory Reachability



Needs to ensure update order is maintained

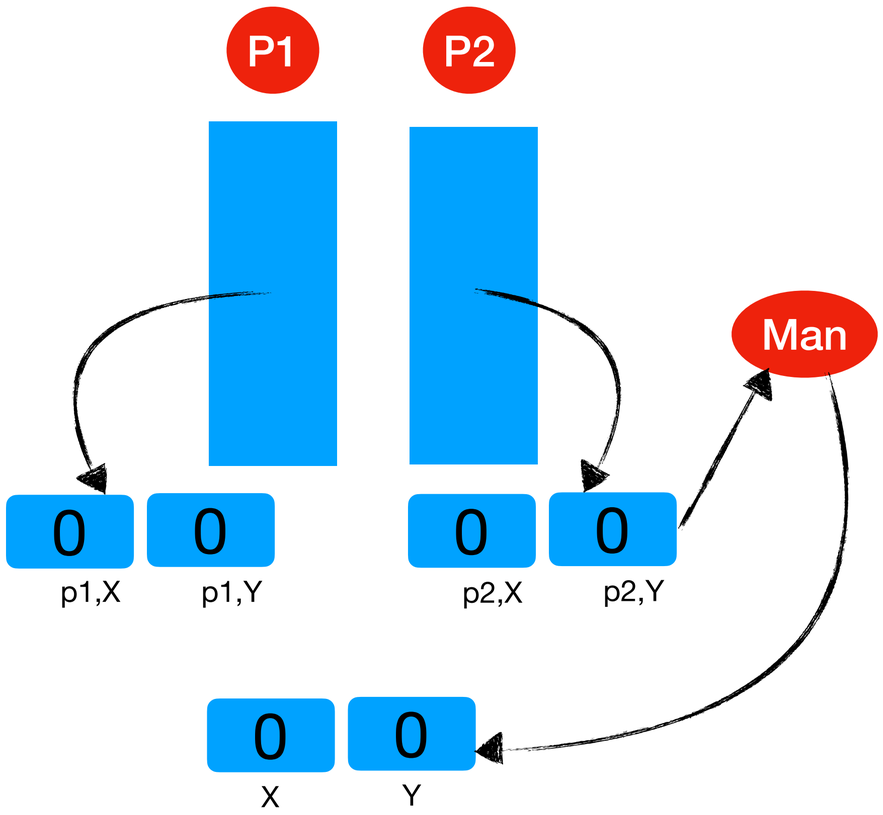
Persistent Memory Reachability



Needs to ensure update order is maintained

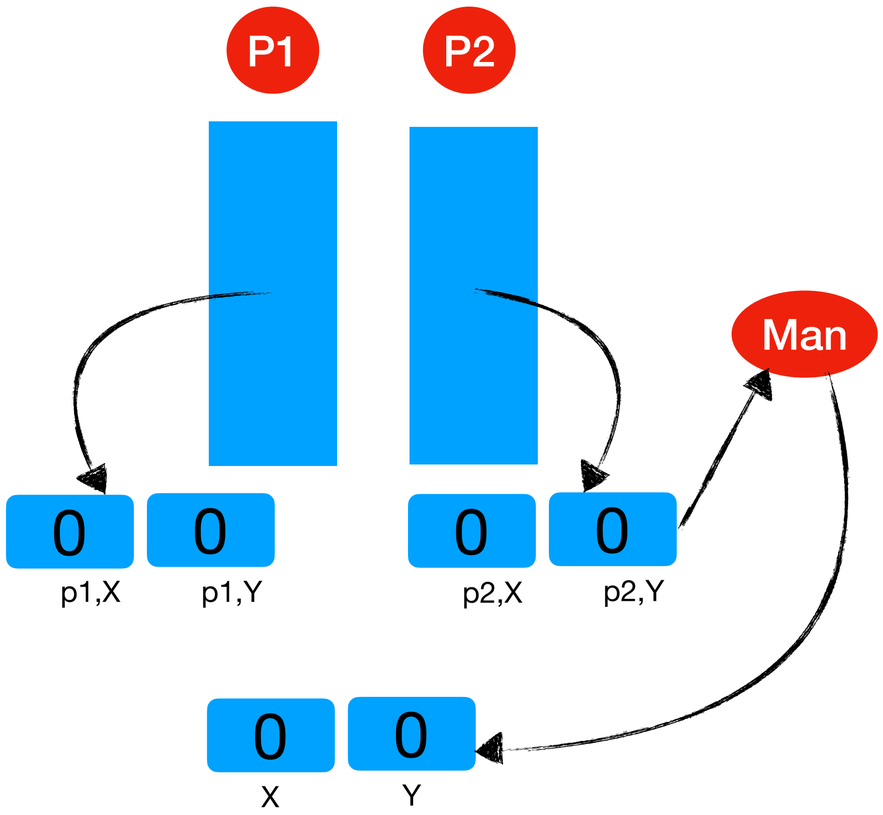
No more updates during a copy

Persistent Memory Reachability



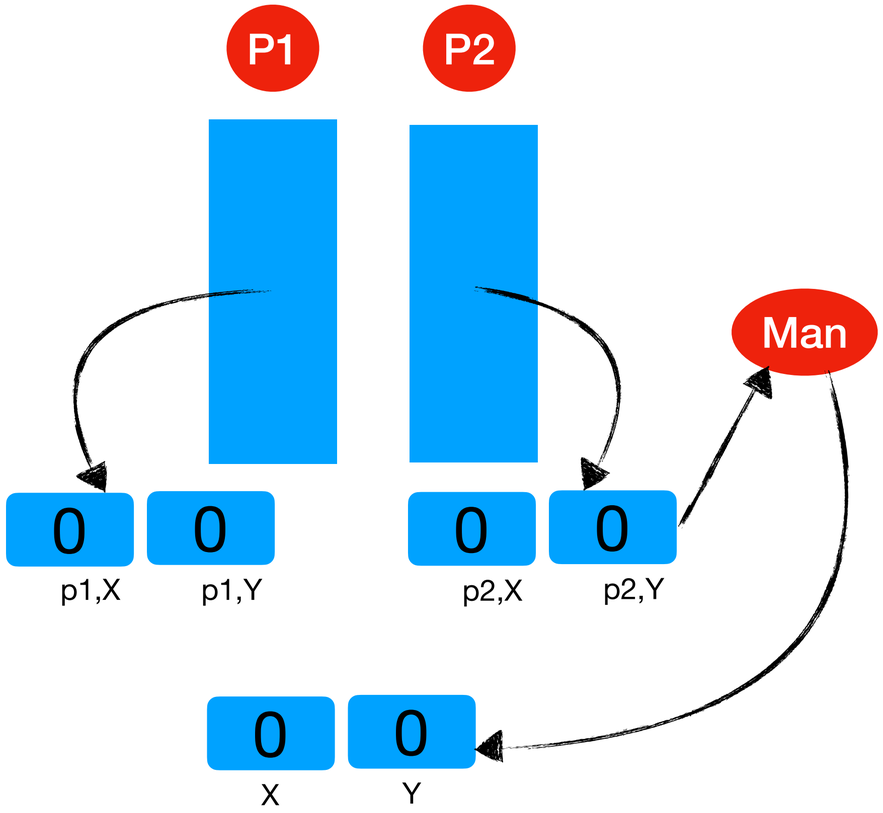
Reads now are from the copy or the main memory

Persistent Memory Reachability



Manager non-deterministically picks a write that will persist

Persistent Memory Reachability



Manager non-deterministically picks a write that will persist

Needs to ensure the value is not over-written

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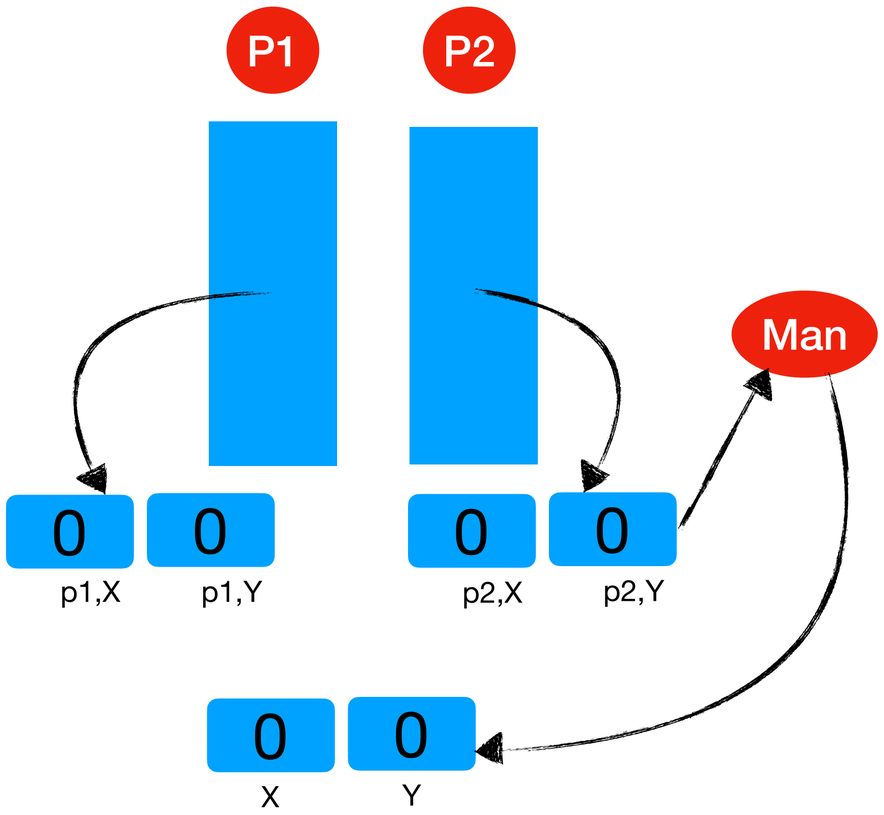

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Frozen write

Spoilers

Spoilers

Frozen write is spoilt by certain bad patterns

Manager tries to avoid these spoilers / bad patterns

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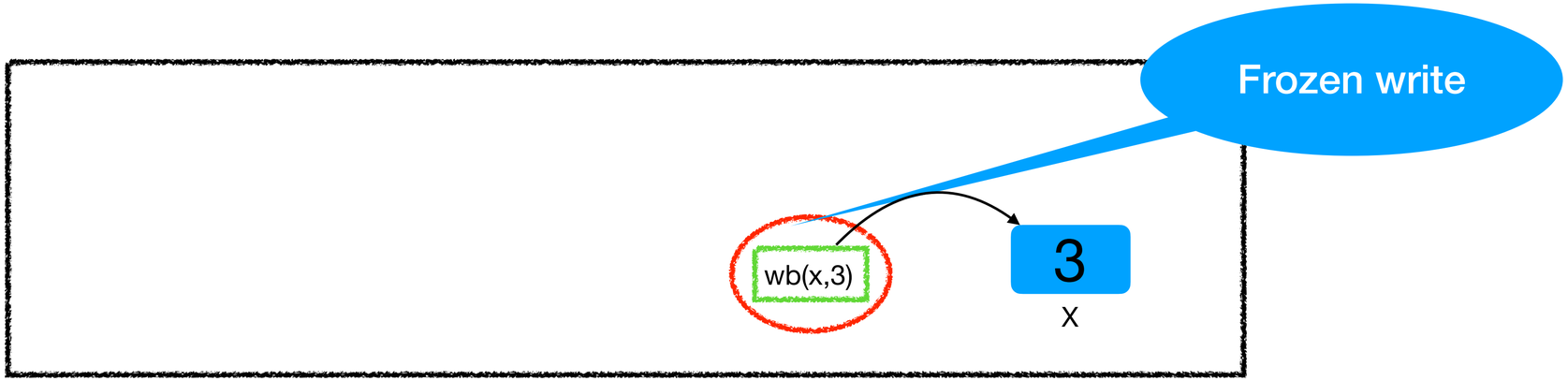

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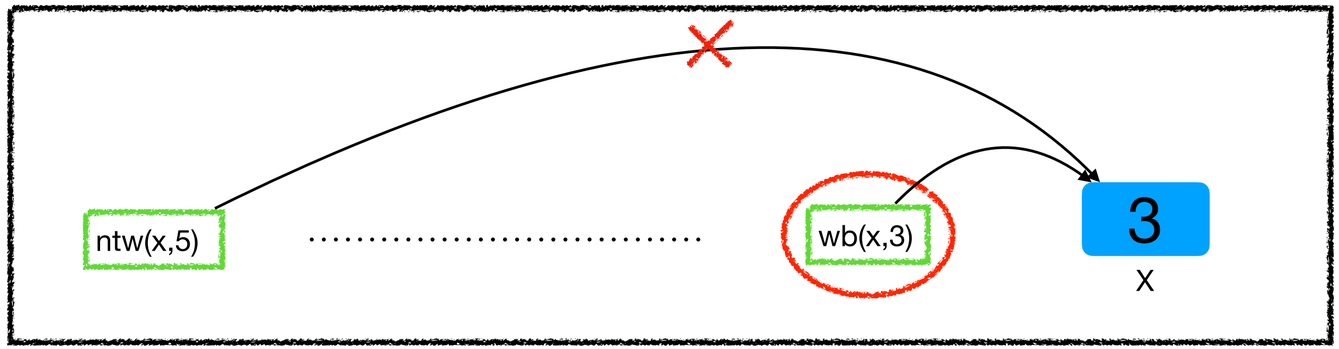

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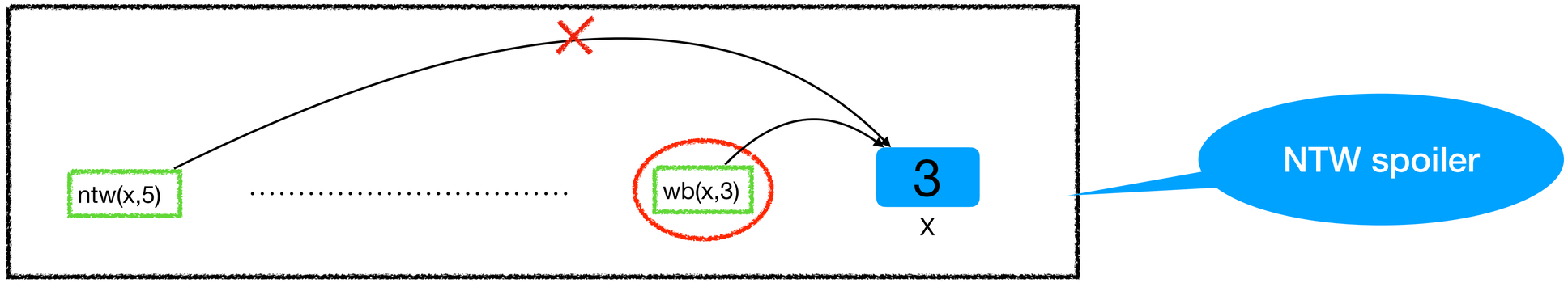

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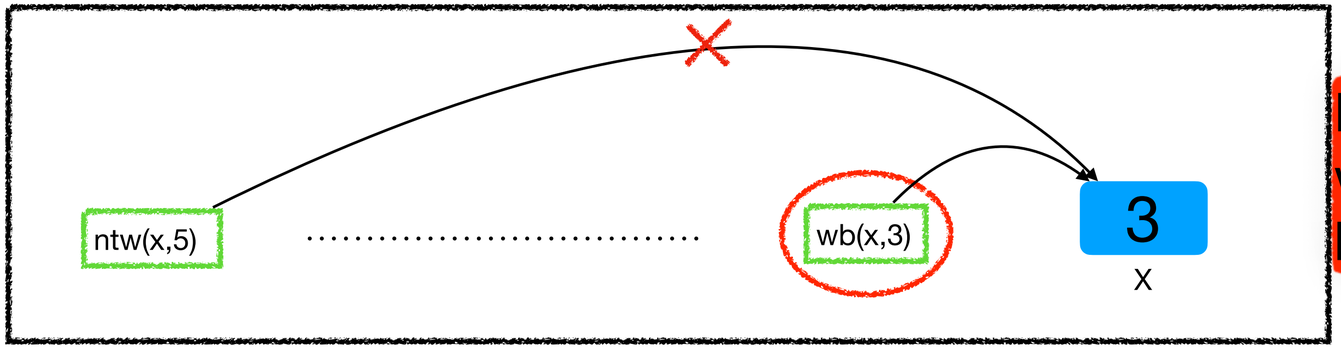

Manager can miss an ntw writes esp if it is followed by a wb write

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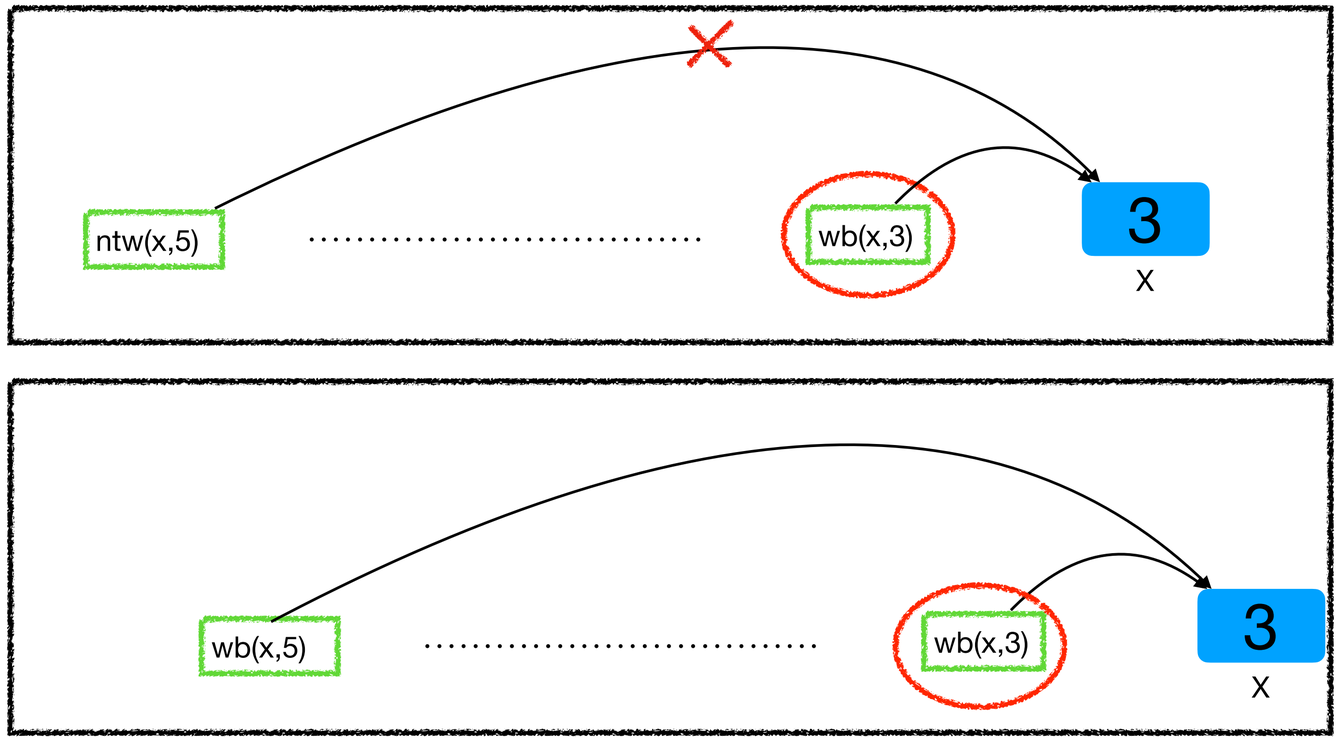

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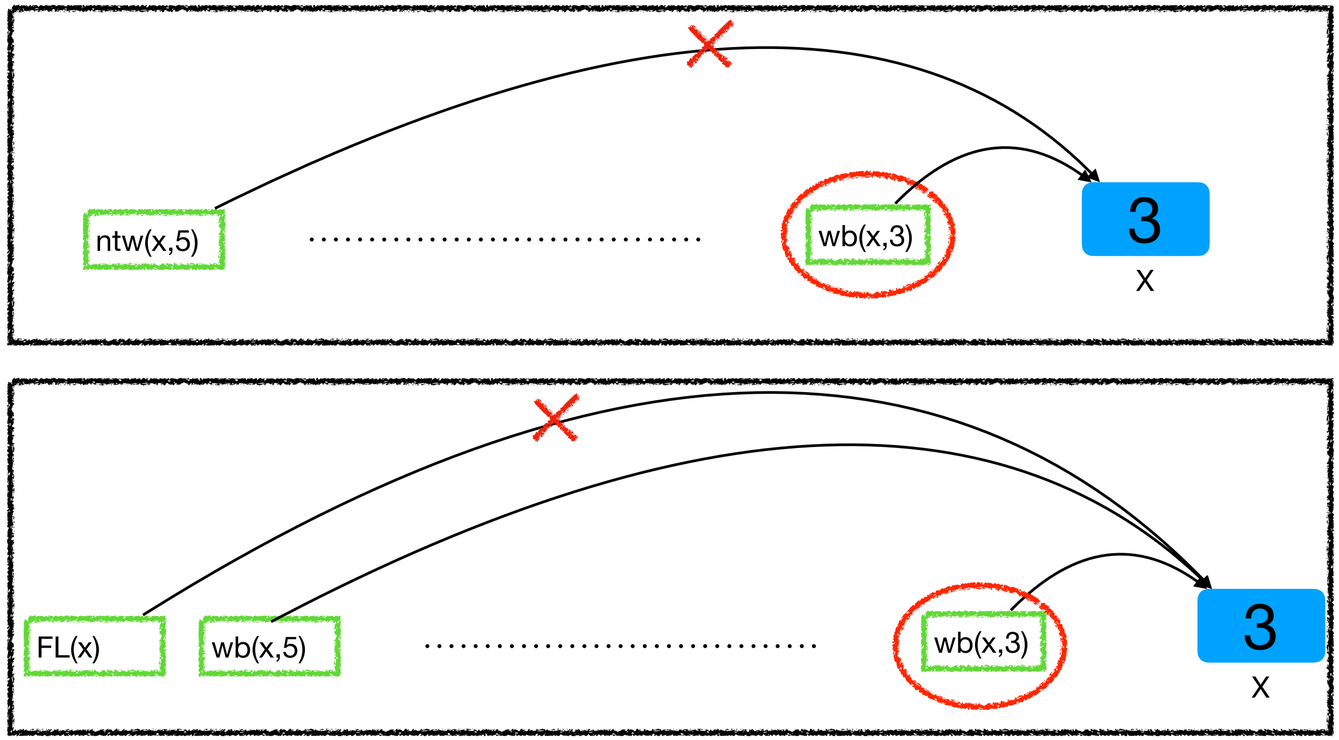

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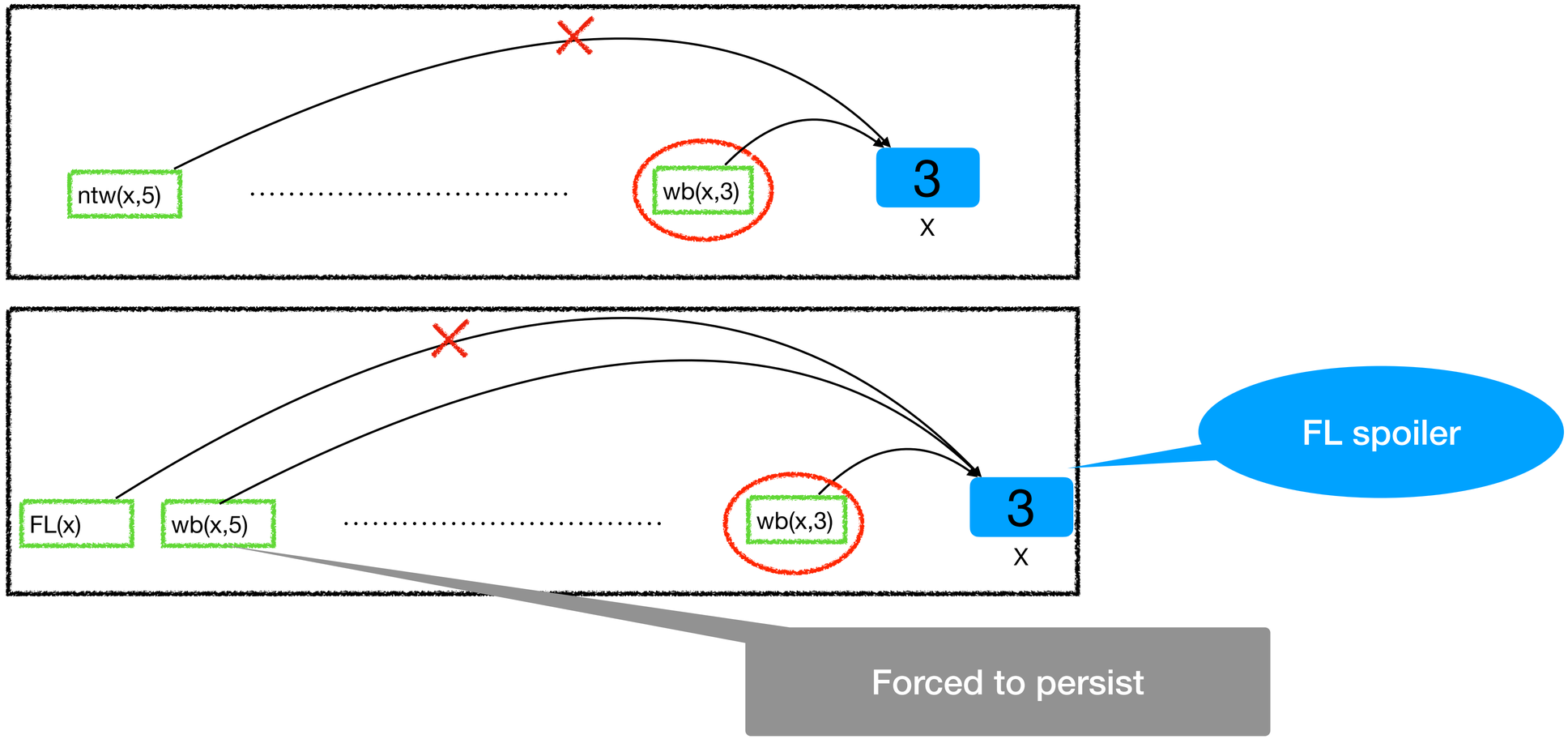

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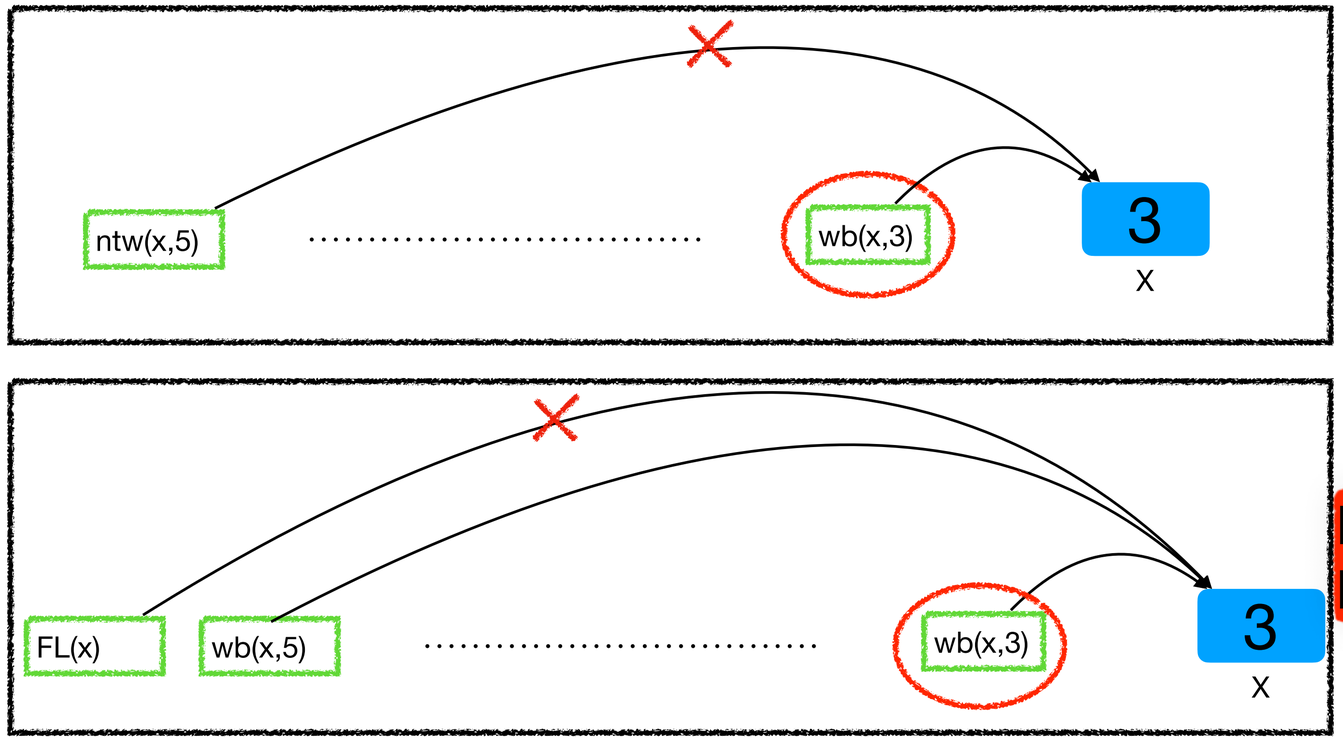

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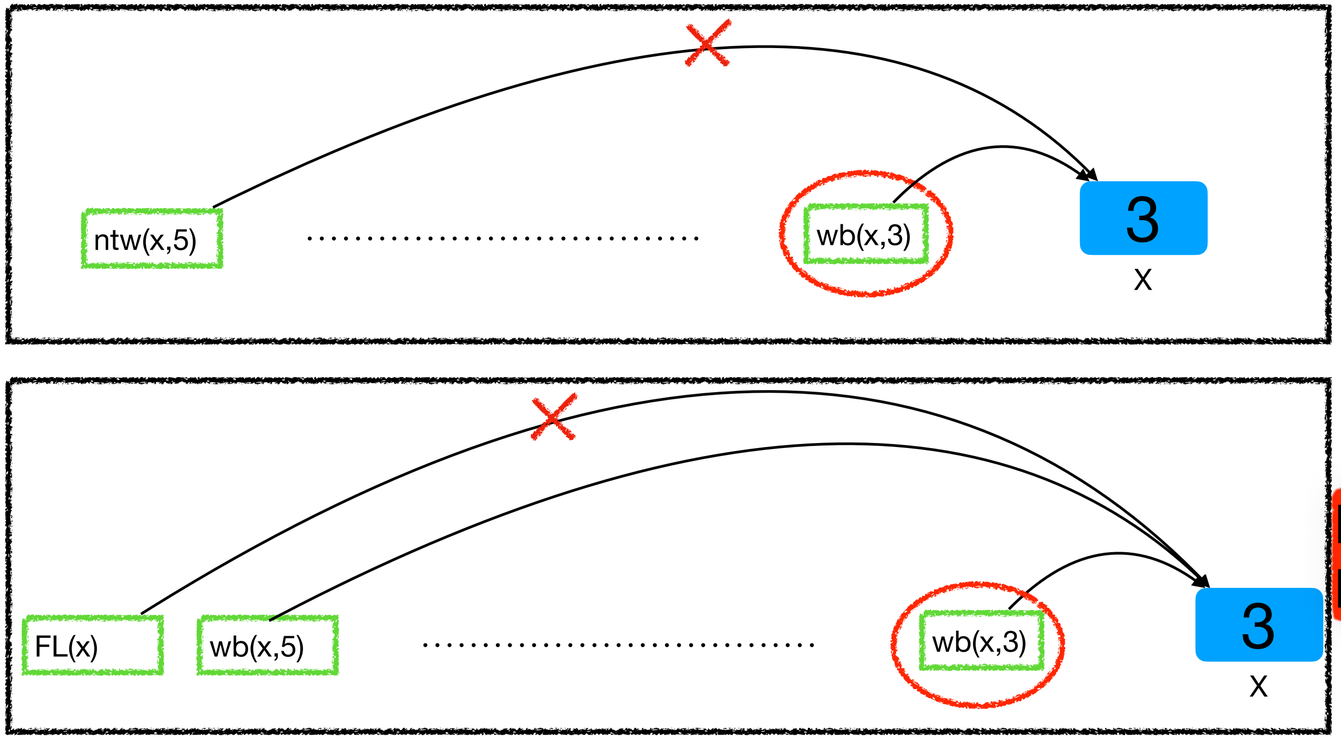

Manager cannot observe Fl operations

There are other spoilers involving Fo, we wont consider them

Detecting Spoilers

Detecting Spoilers

Threads

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- Speculates the position of freeze for each variable
- Tracks potential spoilers to report to the manager

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- Verifies the speculation of the threads
- Ensures that the potential spoilers are never seen

Detecting Spoilers

Threads

Difficult in presence of re-orderings

Speculates the position of freeze for each variable

Tracks potential spoilers to report to the manager

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What About Crash-free Reachability?

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Crash-free reachability is undecidable

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Reduction from well known Post Correspondence Problem

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Crux of the reduction involves ability to implement alternating bit protocol

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Crash-free reachability is undecidable

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Crux of the reduction involves ability to implement alternating bit protocol

Thread 1:

```
1 repeat
2 |   Wb(x, 1);
3 |   Wb(y, 1);
4 until n times;
```

Thread 2:

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1 repeat
2 |   assert(x = 0);
3 |   RMW(x, 1, 0);
4 |   assert(y = 0);
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6 |   assert(x = 0);
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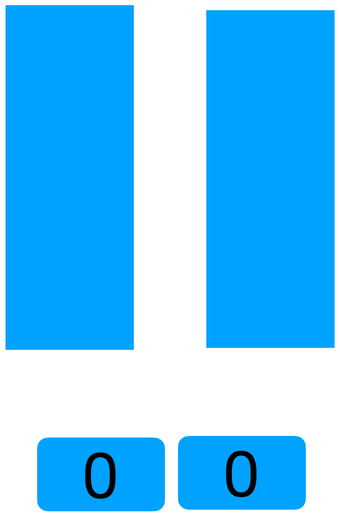

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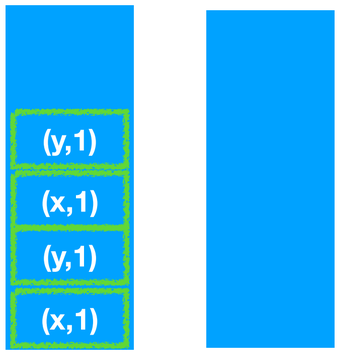

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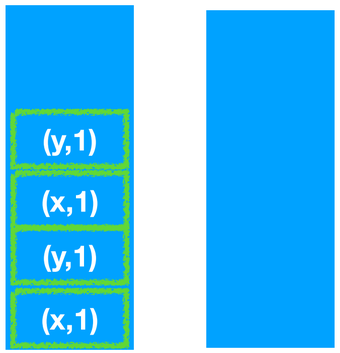

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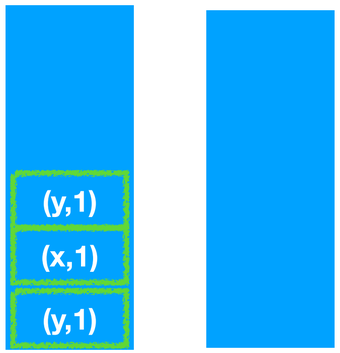

What About Crash-free Reachability?

Crash-free reachability is undecidable

Reduction from well known Post Correspondence Problem

Crux of the reduction involves ability to implement alternating bit protocol

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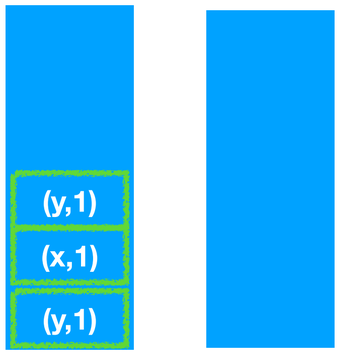

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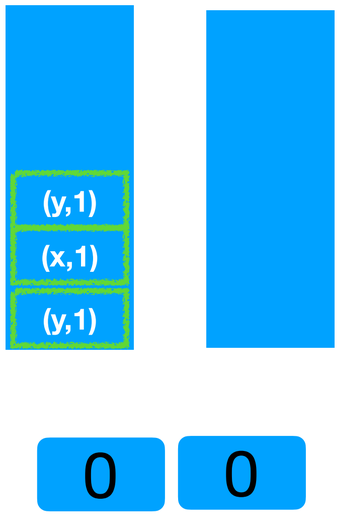

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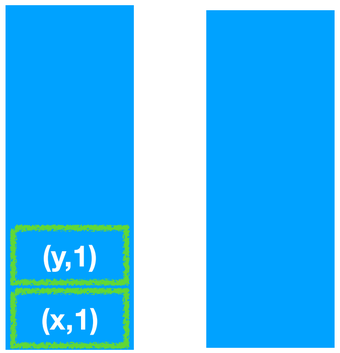

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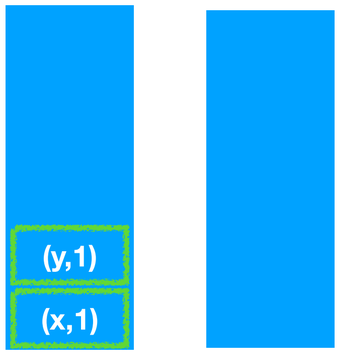

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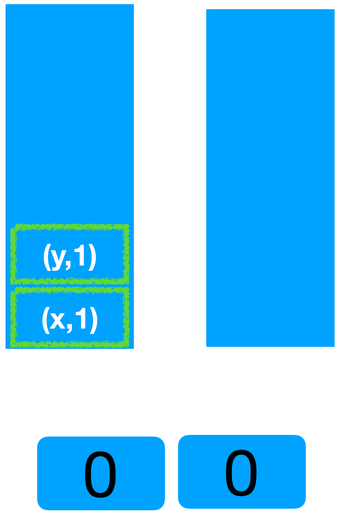

Thread-2 reaches the end only if it did not miss any write

PCP: $U = \{u_1, \ldots u_\ell\} \quad V = \{v_1, \ldots v_\ell\}$

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VERIFYING EX86 WITH PERSISTENCY

All stable processes we shall predict, all unstable processes we shall control - Benjamin Franklin

- Persistent Memory Reachability

- Crash Free Reachability

- Decidable Fragment

Alternation Bounded Reachability

Alternation Bounded Reachability

One source of undecidability is unbounded alternations between ntw and wb writes.

Alternation Bounded Reachability

K Alternation Bounded: An thread execution is k-alternation bounded if the thread alternates between wb and ntw writes at-most k times.

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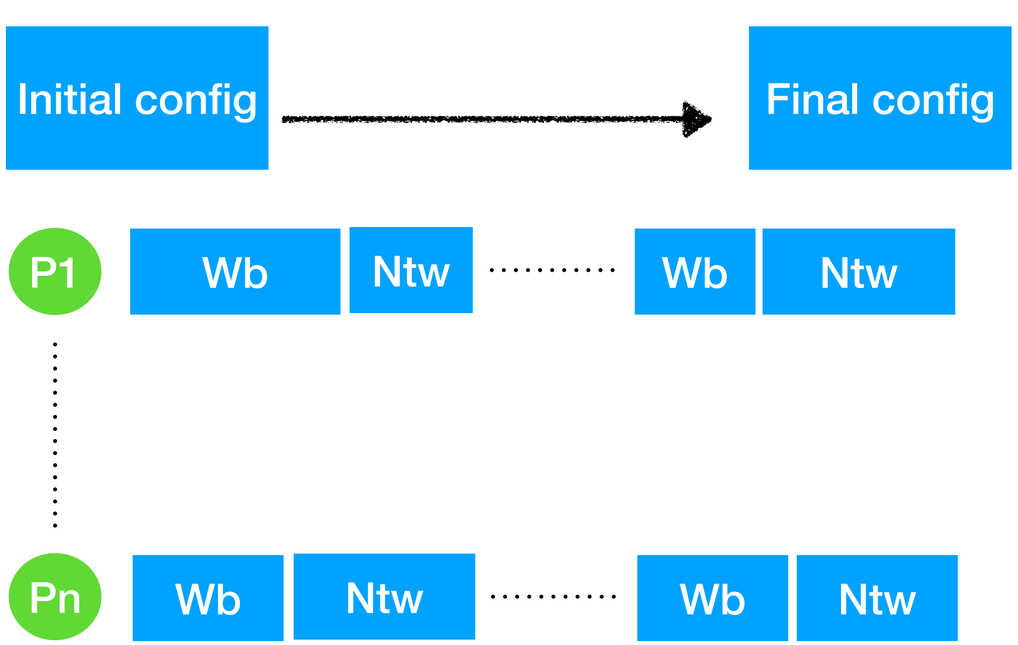

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Decidability

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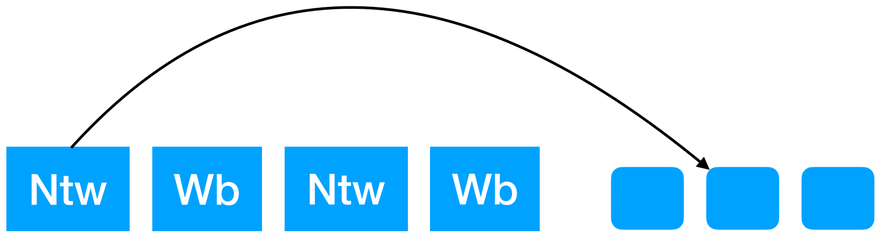
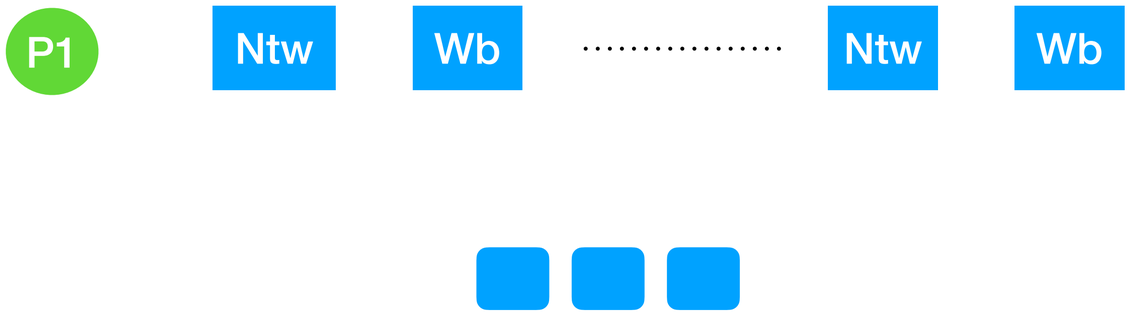


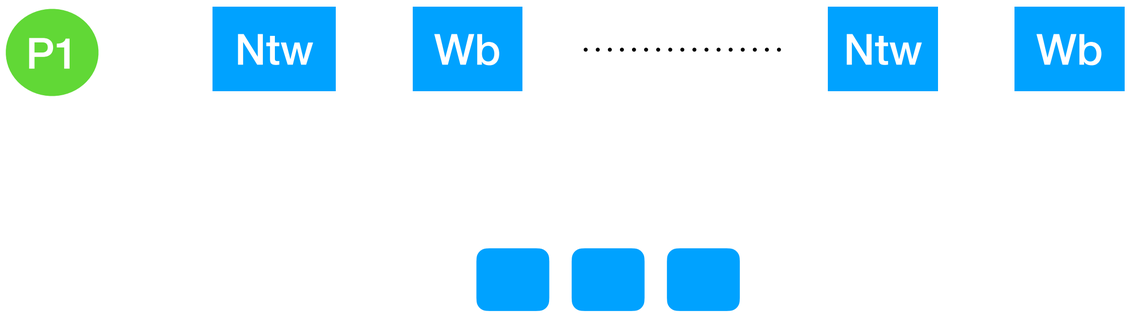
The writes between alternation blocks can re-order

Decidability



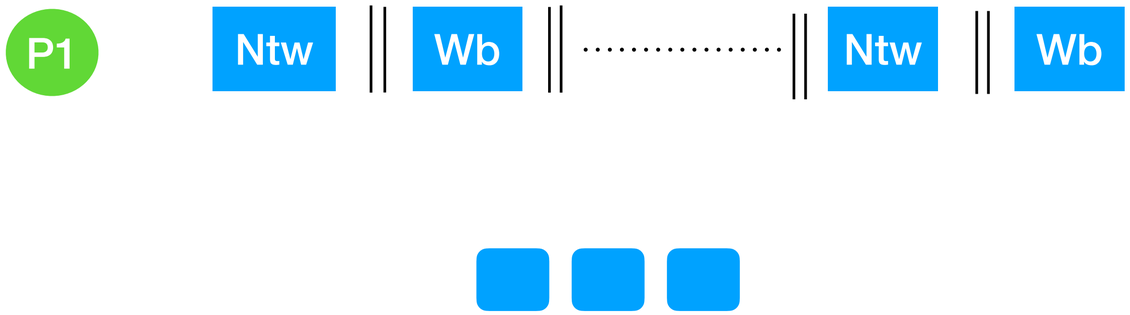
Execution within each block is like TSO or PSO

Decidability



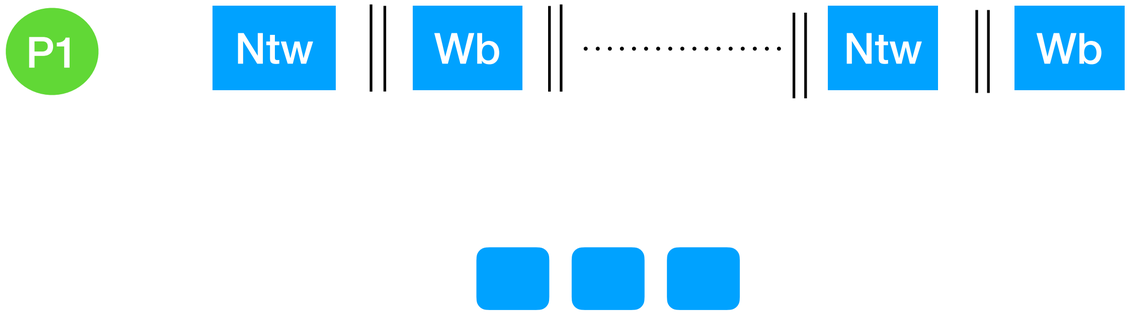
Decidability by reduction to reachability on PSO system

Decidability



Each alternation block is executed in parallel as a PSO thread

Decidability



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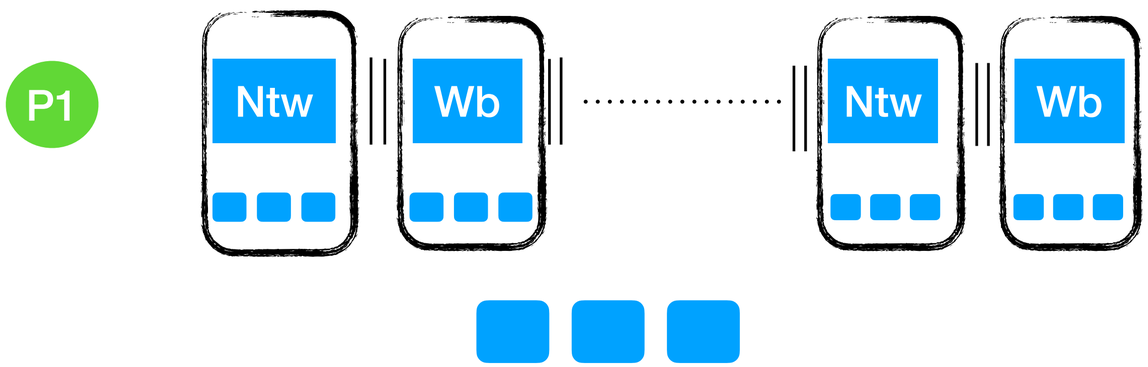
Later blocks depend on earlier blocks

Decidability



Memory is duplicated as per thread and per phase

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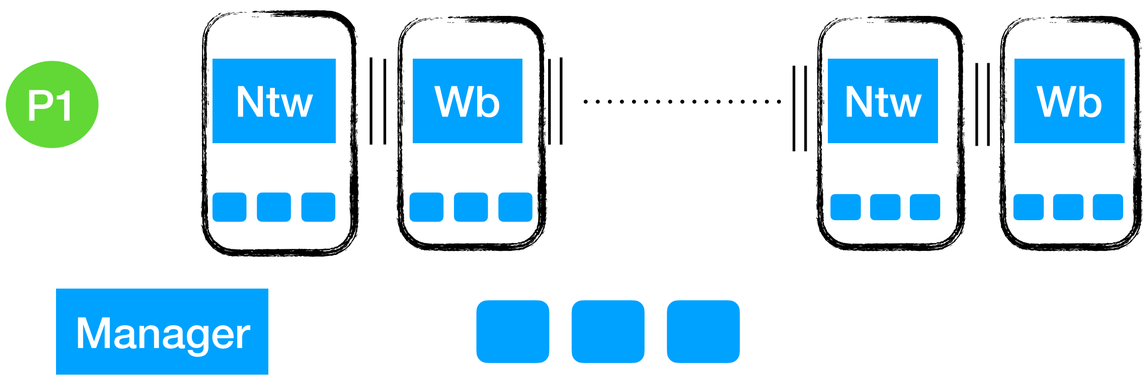

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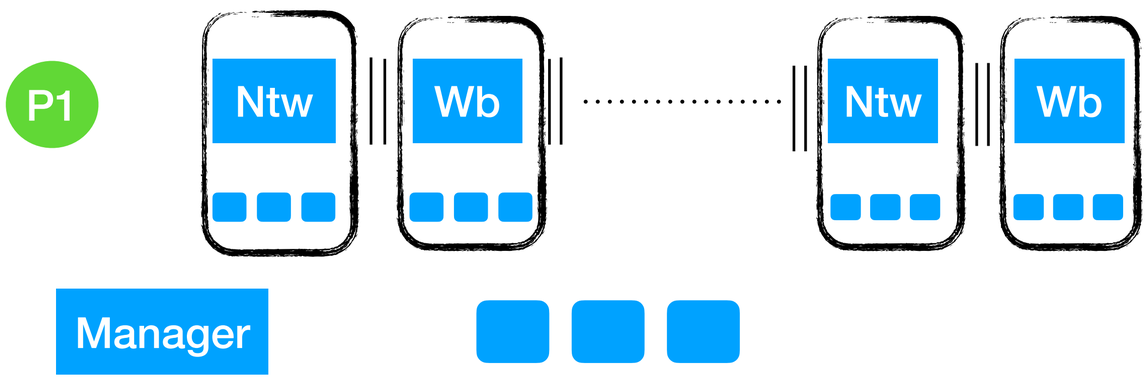
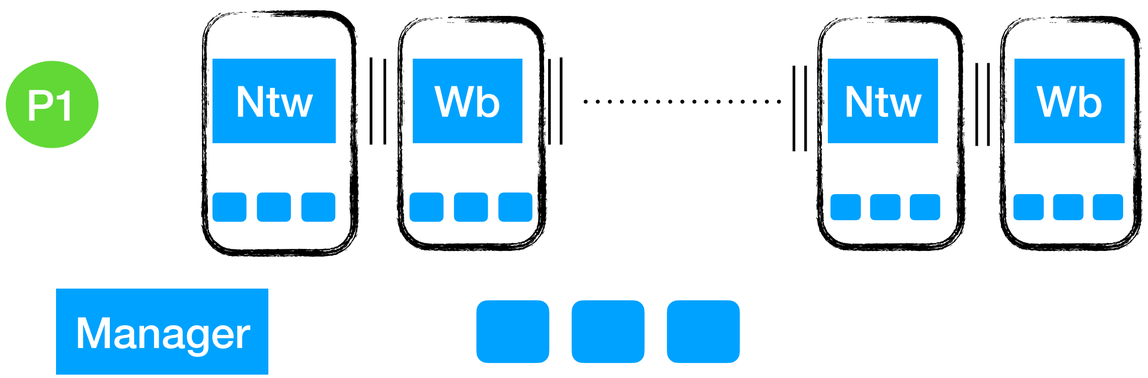


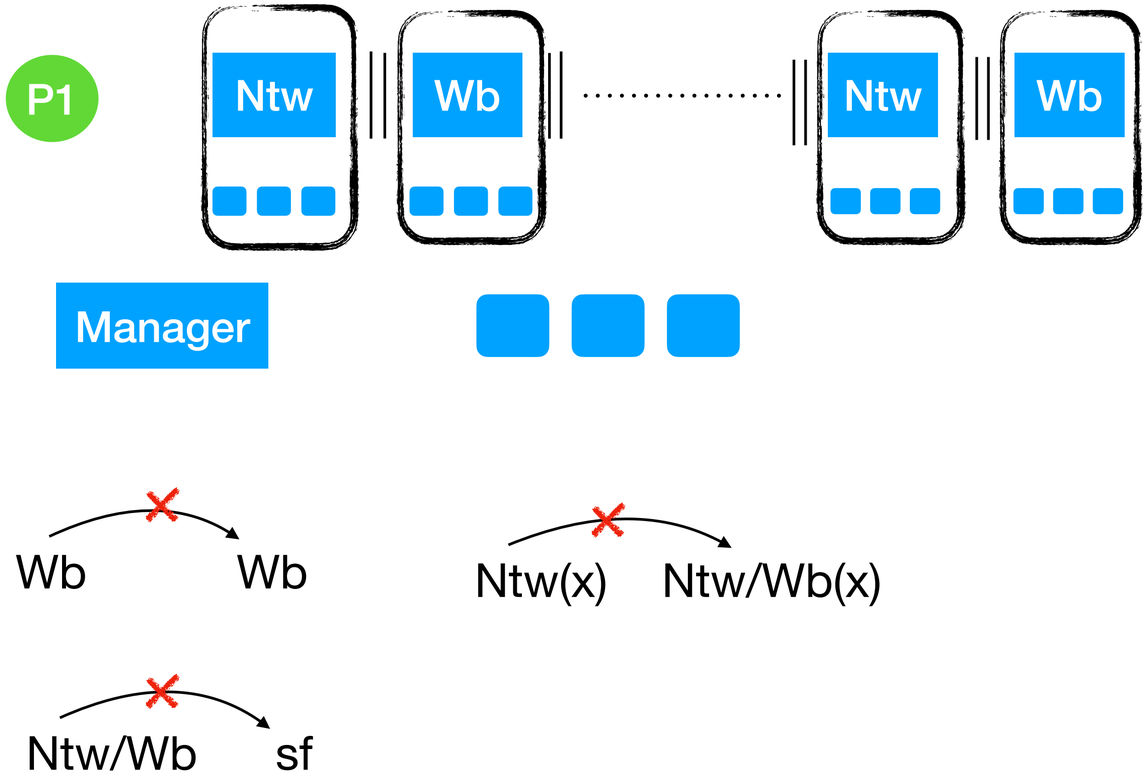
Manager moves the writes to main memory

Decidability



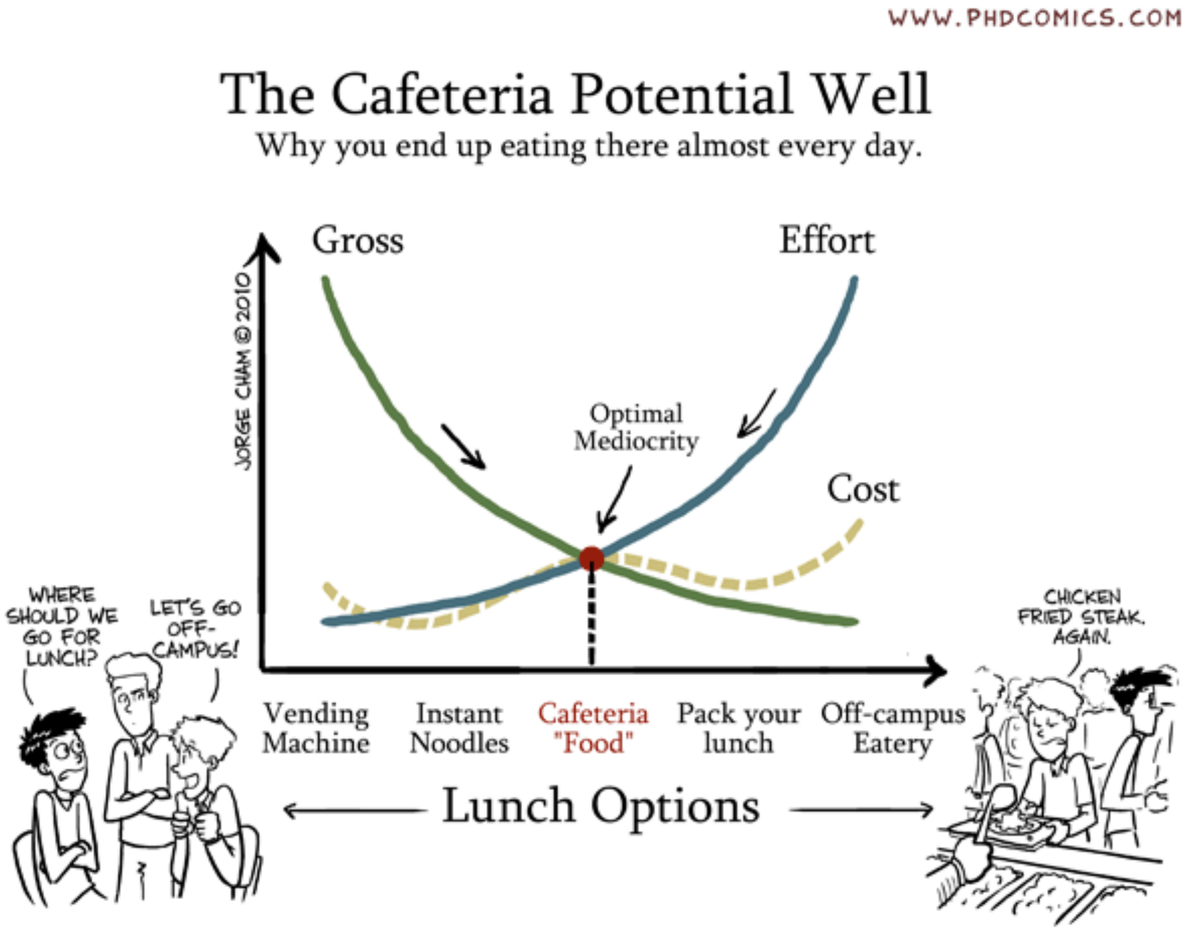
Manager ensures that the semantics is maintained

Decidability



Manager ensures that the semantics is maintained

Thank you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